# PRACTICE QUIZ 03

* Which of the following is true ?

1. In intrinsic Silicon at 300°K the number of free electrons is about equal to the number of Silicon atoms
2. In intrinsic Silicon at 300°K only free electrons can conduct electricity
3. **None of these**
4. In intrinsic Silicon at 300°K there are no free electrons
5. In intrinsic Silicon at 300°K the number of holes is far less than the number of free electrons

* Which of the following is true ?

1. In intrinsic Silicon at 300°K there are some free electrons due to thermal generation
2. In intrinsic Silicon at 300°K both holes and electrons can conduct electricity
3. In intrinsic Silicon at 300°K the number of holes is equal to the number of free electrons
4. In intrinsic Silicon at 300°K the number of holes is far less than the number of Silicon atoms
5. **All of these**

* Which of the following is true ?

1. In intrinsic Silicon at 300°K the number of free electrons is about equal to the number of Silicon atoms
2. **In intrinsic Silicon at 300°K there are some free electrons due to thermal generation**
3. In intrinsic Silicon at 300°K only free electrons can conduct electricity
4. None of these
5. In intrinsic Silicon at 300°K the number of holes is far less than the number of free electrons

* Which of the following is true ?

1. In intrinsic Silicon at 300°K the number of holes is far less than the number of free electrons
2. All of these
3. In intrinsic Silicon at 300°K there are no free electrons
4. In intrinsic Silicon at 300°K the number of free electrons is about equal to the number of Silicon atoms
5. **In intrinsic Silicon at 300°K both holes and electrons can conduct electricity**

* Which of the following is true ?

1. All of these
2. In intrinsic Silicon at 300°K there are no free electrons
3. **In intrinsic Silicon at 300°K the number of holes is far less than the number of Silicon atoms**
4. In intrinsic Silicon at 300°K the number of free electrons is about equal to the number of Silicon atoms
5. In intrinsic Silicon at 300°K only free electrons can conduct electricity

* Which of the following is true ?

1. In intrinsic Silicon at 300°K there are no free electrons
2. In intrinsic Silicon at 300°K the number of holes is far less than the number of free electrons
3. In intrinsic Silicon at 300°K only free electrons can conduct electricity
4. None of these
5. **In intrinsic Silicon at 300°K the number of free electrons is equal to the number of holes**

* Phosphorus (P) and Arsenic (As) are commonly used as acceptor atoms in silicon.

**FALSE (They are donors)**

* Phosphorus (P) and Arsenic (As) are commonly used as donor atoms in silicon.

**TRUE**

* As the reverse bias voltage across a PN junction is decreased, the potential barrier will

1. Stays the same
2. None of these
3. **Decrease**
4. No way to determine
5. Increase

* As the reverse bias across a PN junction is decreased, the potential barrier increases.

**FALSE**

* The diffusion capacitance for a PN junction models the variations in the excess charge stored as carriers are injected across the junction with variations in the forward bias voltage applied.

**TRUE**

* Which of the following is true for a semiconductor doped with Boron at 300°K ?

1. Both the number of holes and the number of free electrons are equal to zero
2. The number of holes is equal to the number of free electrons
3. **The number of holes is greater than the number of free electrons**
4. The number of holes is less than the number of free electrons
5. None of these

* Intrinsic semiconductors are pure, without any impurity atoms added.

**TRUE**

* Which of the following is true for the diffusion capacitance of a PN junction?

1. The amount of charge stored increases as the forward bias increases
2. The capacitance decreases as temperature increases
3. **All of these**
4. The capacitance increases as the forward bias increases
5. The capacitance increases as the mean transit time increases

* Which of the following is true for the diffusion capacitance of a PN junction?

1. **The amount of charge stored increases as the forward bias increases**
2. The capacitance decreases as the mean transit time increases
3. The capacitance decreases as the forward bias increases
4. All of these
5. The capacitance increases as temperature increases

* Which of the following is true for the diffusion capacitance of a PN junction?

1. The capacitance decreases as the mean transit time increases
2. **The capacitance decreases as temperature increases**
3. None of these
4. The amount of charge stored decreases as the forward bias increases
5. The capacitance decreases as the forward bias increases

* Which of the following is true for the diffusion capacitance of a PN junction?

1. **The capacitance increases as the mean transit time increases**
2. The amount of charge stored decreases as the forward bias increases
3. All of these
4. The capacitance increases as temperature increases
5. The capacitance decreases as the forward bias increases

* Which of the following is true for the diffusion capacitance of a PN junction?

1. The amount of charge stored decreases as the forward bias increases
2. **The capacitance increases as the forward bias increases**
3. The capacitance decreases as the mean transit time increases
4. None of these
5. The capacitance increases as temperature increases

* Which of the following is true for the diffusion capacitance of a PN junction?

1. The capacitance increases as temperature increases
2. The capacitance decreases as the mean transit time increases
3. **None of these**
4. The capacitance decreases as the forward bias increases
5. The amount of charge stored decreases as the forward bias increases

* The maximum value for the depletion region capacitance of a reverse biased PN junction occurs when the reverse bias is equal to zero volts.

**TRUE**

* Donor atoms have 3 electrons in their outer most shell.

**FALSE**

* The diffusion capacitance for a PN junction is directly proportional to temperature.

**FALSE**

* In a semiconductor the number of holes multiplied by the number of electrons is equal to a constant even when dopant atoms are added.

**TRUE**

* As the forward bias voltage across a PN junction is decreased, the width of the depletion region will

1. None of these
2. Stays the same
3. **Increase**
4. No way to determine
5. Decrease

* The depletion region surrounding a PN junction contains almost no free electrons and holes.

**TRUE**

* Silicon has approximately 5.0 x 10^22 atoms/cm^3.

**TRUE**

* When a hole moves away from it’s acceptor atom, it leaves behind a negatively charged ion.

**TRUE**

* Which of the following is true ?

1. **All of these**
2. Boron is often used as a P-type dopant in Silicon
3. Phosphorus is often used as an N-type dopant in Silicon
4. Carbon is never used as a dopant in Silicon
5. Arsenic is often used as an N-type dopant in Silicon

* Which of the following is true ?

1. Carbon is often used as a P-type dopant in Silicon
2. Phosphorus is often used as a P-type dopant in Silicon
3. Boron is often used as an N-type dopant in Silicon
4. **Arsenic is often used as an N-type dopant in Silicon**
5. None of these

* Which of the following is true ?

1. Arsenic is often used as a P-type dopant in Silicon
2. Carbon is often used as a P-type dopant in Silicon
3. **Boron is often used as a P-type dopant in Silicon**
4. Phosphorus is often used as a P-type dopant in Silicon
5. None of these

* Which of the following is true ?

1. All of these
2. **Carbon is never used as a dopant in Silicon**
3. Boron is often used as an N-type dopant in Silicon
4. Arsenic is often used as a P-type dopant in Silicon
5. Phosphorus is often used as a P-type dopant in Silicon

* Which of the following is true ?

1. Carbon is often used as a P-type dopant in Silicon
2. All of these
3. **Phosphorus is often used as an N-type dopant in Silicon**
4. Boron is often used as an N-type dopant in Silicon
5. Arsenic is often used as a P-type dopant in Silicon

* Which of the following is true ?

1. Arsenic is often used as a P-type dopant in Silicon
2. **None of these**
3. Carbon is often used as an N-type dopant in Silicon
4. Boron is often used as an N-type dopant in Silicon
5. Phosphorus is often used as a P-type dopant in Silicon

* When a free electron moves away from it’s donor atom, it leaves behind a positively charged ion.

**TRUE**

* Acceptor atoms have 3 electrons in their outer most shell.

**TRUE**

* When P-type Silicon is brought into contact with N-type Silicon to form a PN Junction :

1. Holes diffuse from the P side to the N side, and electrons diffuse from the N side to the P side
2. The donor and acceptor atoms near the junction are ionized, leaving behind fixed charge
3. **All of these**
4. The area around the junction is depleted of free electrons and holes
5. The separation of charge causes an electric field which opposes the diffusion of carriers

* When P-type Silicon is brought into contact with N-type Silicon to form a PN Junction :

1. The donor and acceptor atoms near the junction are free to conduct electricity
2. The separation of charge causes an electric field which assists the diffusion of carriers
3. All of these
4. The area around the junction is depleted of immobile ions
5. **Holes diffuse from the P side to the N side, and electrons diffuse from the N side to the P side**

* When P-type Silicon is brought into contact with N-type Silicon to form a PN Junction :

1. The separation of charge causes an electric field which assists the diffusion of carriers
2. **The area around the junction is depleted of free electrons and holes**
3. The donor and acceptor atoms near the junction are free to conduct electricity
4. None of these
5. Holes diffuse from the N side to the P side, and electrons diffuse from the P side to the N side

* When P-type Silicon is brought into contact with N-type Silicon to form a PN Junction :

1. The area around the junction is depleted of immobile ions
2. Holes diffuse from the N side to the P side, and electrons diffuse from the P side to the N side
3. The donor and acceptor atoms near the junction are free to conduct electricity
4. None of these
5. **The separation of charge causes an electric field which opposes the diffusion of carriers**

* When P-type Silicon is brought into contact with N-type Silicon to form a PN Junction :

1. Holes diffuse from the N side to the P side, and electrons diffuse from the P side to the N side
2. **The donor and acceptor atoms near the junction are ionized, leaving behind fixed charge**
3. The area around the junction is depleted of immobile ions
4. The separation of charge causes an electric field which assists the diffusion of carriers
5. All of these

* When P-type Silicon is brought into contact with N-type Silicon to form a PN Junction :

1. Holes diffuse from the N side to the P side, and electrons diffuse from the P side to the N side
2. The donor and acceptor atoms near the junction are free to conduct electricity
3. The separation of charge causes an electric field which assists the diffusion of carriers
4. **None of these**
5. The area around the junction is depleted of immobile ions

* The charge stored in the depletion region decreases as the reverse bias voltage increases, which causes a capacitance.

**False**

* For abrupt step PN junctions, the depletion capacitance depends on the cube root of the reverse bias voltage.

**FALSE**

* Which of the following is true ?

1. In doped Silicon at 300°K nearly all the acceptor atoms have “accepted” an electron, creating a hole
2. In doped Silicon at 300°K nearly all the donor atoms have “donated” a free electron
3. **All of these**
4. In doped Silicon at 300°K nearly all the acceptor atoms are negatively charged immobile ions
5. In doped Silicon at 300°K nearly all the donor atoms are positively charged immobile ions

* Which of the following is true ?

1. In doped Silicon at 300°K nearly all the acceptor atoms are positively charged immobile ions
2. In doped Silicon at 300°K nearly all the donor atoms are negatively charged immobile ions
3. In doped Silicon at 300°K nearly all the donor atoms have “donated” a hole
4. **In doped Silicon at 300°K nearly all the acceptor atoms have “accepted” an electron, creating a hole**
5. None of these

* Which of the following is true ?

1. All of these
2. **In doped Silicon at 300°K nearly all the donor atoms have “donated” a free electron**
3. In doped Silicon at 300°K nearly all the donor atoms are negatively charged immobile ions
4. In doped Silicon at 300°K nearly all the acceptor atoms have “accepted” a hole
5. In doped Silicon at 300°K nearly all the acceptor atoms are positively charged immobile ions

* Which of the following is true ?

1. In doped Silicon at 300°K nearly all the acceptor atoms are positively charged immobile ions
2. In doped Silicon at 300°K nearly all the acceptor atoms have “accepted” a hole
3. **In doped Silicon at 300°K nearly all the donor atoms are positively charged immobile ions**
4. In doped Silicon at 300°K nearly all the donor atoms have “donated” a hole
5. All of these

* Which of the following is true ?

1. In doped Silicon at 300°K nearly all the donor atoms are negatively charged immobile ions
2. None of these
3. In doped Silicon at 300°K nearly all the donor atoms have “donated” a hole
4. In doped Silicon at 300°K nearly all the acceptor atoms have “accepted” a hole
5. **In doped Silicon at 300°K nearly all the acceptor atoms are negatively charged immobile ions**

* In doped Silicon at 300°K nearly all the acceptor atoms have “accepted” a hole

1. In doped Silicon at 300°K nearly all the donor atoms have “donated” a hole
2. In doped Silicon at 300°K nearly all the donor atoms are negatively charged immobile ions
3. In doped Silicon at 300°K nearly all the acceptor atoms have “accepted” a hole
4. **None of these**
5. In doped Silicon at 300°K nearly all the acceptor atoms are positively charged immobile ions

* In a semiconductor doped with donor atoms, the number of holes is much higher than the number of electrons.

**FALSE**

* Diffusion refers to the fundamental property in nature that most things tend to move from areas where they are in low concentration to areas where they are in high concentration.

**FALSE**

* Silicon has approximately 1.5 x 10^10 atoms/cm^3.

**FALSE**

* As the forward bias voltage across a PN junction is increased, the potential barrier will

1. No way to determine
2. **Decrease**
3. Stays the same
4. None of these
5. Increase

* For linearly graded PN junctions, the depletion capacitance depends on the cube root of the reverse bias voltage.

**TRUE**

* In a semiconductor doped with donor atoms, the number of electrons is much higher than the number of holes.

**TRUE**

* As the forward bias voltage across a PN junction is decreased, the diffusion capacitance will

1. **Decrease**
2. None of these
3. Increase
4. No way to determine
5. Stays the same

* As the reverse bias across a PN junction is increased, the width of the depletion region decreases.

**FALSE**

* Which of the following is true ?

1. Phosphorus has 5 electrons in its outermost shell
2. **All of these**
3. Silicon has 4 electrons in its outermost shell
4. Boron has 3 electrons in its outermost shell
5. Arsenic has 5 electrons in its outermost shell

* Which of the following is true ?

1. Arsenic has 4 electrons in its outermost shell
2. Silicon has 3 electrons in its outermost shell
3. **Phosphorus has 5 electrons in its outermost shell**
4. All of these
5. Boron has 5 electrons in its outermost shell

* Which of the following is true ?

1. Arsenic has 4 electrons in its outermost shell
2. Silicon has 5 electrons in its outermost shell
3. **Boron has 3 electrons in its outermost shell**
4. Phosphorus has 4 electrons in its outermost shell
5. None of these

* Which of the following is true ?

1. Arsenic has 3 electrons in its outermost shell
2. Phosphorus has 3 electrons in its outermost shell
3. All of these
4. **Silicon has 4 electrons in its outermost shell**
5. Boron has 5 electrons in its outermost shell

* Which of the following is true ?

1. Boron has 4 electrons in its outermost shell
2. **Arsenic has 5 electrons in its outermost shell**
3. Phosphorus has 3 electrons in its outermost shell
4. Silicon has 5 electrons in its outermost shell
5. None of these

* Which of the following is true ?

1. Phosphorus has 3 electrons in its outermost shell
2. **None of these**
3. Arsenic has 4 electrons in its outermost shell
4. Boron has 5 electrons in its outermost shell
5. Silicon has 5 electrons in its outermost shell

* Doped semiconductors have controlled amounts of impurity atoms added to vary their resistance.

**TRUE**

* The p-side of a PN junction is called the cathode, and the n-side of the PN junction is called the anode.

**FALSE**

* Silicon has 4 electrons in its outermost shell, which form covalent bonds with other atoms to form a crystal.

**TRUE**

* Which of the following is true for the depletion region surrounding a PN junction?

1. **All of these**
2. In the depletion region there are immobile ions which cause a separation of charge
3. In the depletion region the amount of charge stored varies with the applied bias, causing a capacitance
4. In the depletion region there are almost no free electrons and holes
5. In the depletion region there is an electric field, which creates a barrier voltage

* Which of the following is true for the depletion region surrounding a PN junction?

1. In the depletion region the amount of charge stored stays constant as the bias is varied
2. In the depletion region there are almost no immobile ions
3. None of these
4. **In the depletion region there are immobile ions which cause a separation of charge**
5. In the depletion region there is zero electric field

* Which of the following is true for the depletion region surrounding a PN junction?

1. **In the depletion region the amount of charge stored varies with the applied bias, causing a capacitance**
2. In the depletion region there is zero electric field
3. In the depletion region there are almost no immobile ions
4. In the depletion region there are free electrons and holes which cause a separation of charge
5. None of these

* Which of the following is true for the depletion region surrounding a PN junction?

1. In the depletion region there is zero electric field
2. All of these
3. In the depletion region the amount of charge stored stays constant as the bias is varied
4. **In the depletion region there are almost no free electrons and holes**
5. In the depletion region there are free electrons and holes which cause a separation of charge

* Which of the following is true for the depletion region surrounding a PN junction?

1. **In the depletion region there is an electric field, which creates a barrier voltage**
2. All of these
3. In the depletion region there are free electrons and holes which cause a separation of charge
4. In the depletion region there are almost no immobile ions
5. In the depletion region the amount of charge stored stays constant as the bias is varied

* Which of the following is true for the depletion region surrounding a PN junction?

1. **None of these**
2. In the depletion region there are free electrons and holes which cause a separation of charge
3. In the depletion region there are almost no immobile ions
4. In the depletion region there is zero electric field
5. In the depletion region the amount of charge stored stays constant as the bias is varied

* Which of the following is true for a semiconductor doped with Arsenic at 300°K ?

1. Both the number of holes and the number of free electrons are equal to zero
2. The number of holes is greater than the number of free electrons
3. **The number of holes is less than the number of free electrons**
4. The number of holes is equal to the number of free electrons
5. All of these

* Which of the following is true for the depletion region capacitance of a PN junction?

1. The capacitance depends on the cube root of the reverse bias for a linearly graded junction
2. The capacitance decreases as the reverse bias increases
3. **All of these**
4. The capacitance depends on the square root of the reverse bias for an abrupt step junction
5. The amount of charge stored increases as the reverse bias increases

* Which of the following is true for the depletion region capacitance of a PN junction?

1. The capacitance decreases as the reverse bias decreases
2. The amount of charge stored decreases as the reverse bias increases
3. The capacitance depends on the square root of the reverse bias for a linearly graded junction
4. **The capacitance depends on the square root of the reverse bias for an abrupt step junction**
5. None of these

* Which of the following is true for the depletion region capacitance of a PN junction?

1. **The capacitance depends on the cube root of the reverse bias for a linearly graded junction**
2. All of these
3. The capacitance depends on the cube root of the reverse bias for an abrupt step junction
4. The amount of charge stored decreases as the reverse bias increases
5. The capacitance decreases as the reverse bias decreases

* Which of the following is true for the depletion region capacitance of a PN junction?

1. The capacitance depends on the square root of the reverse bias for a linearly graded junction
2. The capacitance decreases as the reverse bias decreases
3. The capacitance depends on the cube root of the reverse bias for an abrupt step junction
4. None of these
5. **The amount of charge stored increases as the reverse bias increases**

* Which of the following is true for the depletion region capacitance of a PN junction?

1. **The capacitance decreases as the reverse bias increases**
2. The capacitance depends on the cube root of the reverse bias for an abrupt step junction
3. All of these
4. The amount of charge stored decreases as the reverse bias increases
5. The capacitance depends on the square root of the reverse bias for a linearly graded junction

* Which of the following is true for the depletion region capacitance of a PN junction?

1. The capacitance decreases as the reverse bias decreases
2. The capacitance depends on the square root of the reverse bias for a linearly graded junction
3. The amount of charge stored decreases as the reverse bias increases
4. The capacitance depends on the cube root of the reverse bias for an abrupt step junction
5. **None of these**

* The “built-in voltage” for a PN junction goes up as the doping levels increase.

**TRUE**

* The “built-in voltage” for a PN junction goes down as the doping levels increase.

**FALSE**

* Intrinsic semiconductors have controlled amounts of impurity atoms added to vary their resistance.

**FALSE**

* The separation of charge caused by the immobile ions in the depletion region surrounding a PN junction creates an electric field, which assists the further diffusion of electrons and holes.

**FALSE**

* When silicon is doped with acceptor atoms, this increases the number of holes.

**TRUE**

* The reverse breakdown voltage of a PN junction increases as the doping levels increase.

**FALSE**

* As the forward bias voltage across a PN junction is increased, the diffusion capacitance will

1. None of these
2. Decrease
3. No way to determine
4. Stays the same
5. **Increase**

* If a semiconductor is doped with donor atoms, then:

1. There could be either more holes, or more free electrons
2. There are the same number of free electrons and holes
3. None of these
4. There are many more holes than free electrons
5. **There are many more free electrons than holes**

* The intrinsic carrier concentration for silicon is about 1.5 x 10^10/cm^3 at room temperature (300°K).

**TRUE**

* Which of the following is true for an intrinsic semiconductor at 300°K ?

1. Both the number of holes and the number of free electrons are equal to zero
2. None of these
3. The number of holes is less than the number of free electrons
4. The number of holes is greater than the number of free electrons
5. **The number of holes is equal to the number of free electrons**

* The depletion region capacitance increases linearly as the reverse bias voltage is decreased.

**FALSE**

* Lightly doped PN junctions break down at higher reverse voltages than heavily doped PN junctions.

**TRUE**

* Silicon has 5 electrons in its outermost shell, which form covalent bonds with other atoms to form a crystal.

**FALSE**

* When p-type silicon is brought into contact with n-type silicon, holes diffuse from the P side to the N side, and electrons diffuse from the N side to the P side.

**TRUE**

* The depletion region capacitance decreases linearly as the reverse bias voltage is increased.

**FALSE**

* Both holes and electrons leave behind mobile ions when they conduct electricity.

**FALSE**

* In a semiconductor doped with acceptor atoms, the number of holes is much higher than the number of electrons.

**TRUE**

* The Avalanche effect typically causes the reverse breakdown of PN junctions which break down at voltages > 7V.

**TRUE**

* The intrinsic carrier concentration for silicon increases as temperature increases.

**TRUE**

* As the forward bias across a PN junction is decreased, the potential barrier decreases.

**FALSE**

* The intrinsic carrier concentration for silicon stays approximately constant as temperature increases.

**FALSE**

* When p-type silicon is brought into contact with metal, a PN junction is formed.

**FALSE**

* Which of the following is true for an intrinsic semiconductor at 0°K ?

1. The number of holes is equal to the number of free electrons
2. The number of holes is greater than the number of free electrons
3. **Both the number of holes and the number of free electrons are equal to zero**
4. All of these
5. The number of holes is less than the number of free electrons

* The intrinsic carrier concentration for silicon is about 5.0 x 10^22/cm^3 at room temperature (300°K).

**FALSE**

* Diffusion refers to the fundamental property in nature that most things tend to move from areas where they are in high concentration to areas where they are in low concentration.

**TRUE**

* The diffusion capacitance for a PN junction is inversely proportional to temperature.

**TRUE**

* Donor atoms have 5 electrons in their outer most shell.

**TRUE**

* The diffusion capacitance for a PN junction is inversely proportional to the average time it takes for a carrier to recombine after it crosses the junction.

**FALSE**

* Silicon is the most widely used semiconductor today.

**TRUE**

* As the reverse bias voltage across a PN junction is increased, the depletion capacitance will

1. Stays the same
2. No way to determine
3. Increase
4. None of these
5. **Decrease**

* Heavily doped PN junctions break down at higher reverse voltages than lightly doped PN junctions.

**FALSE**

* As the reverse bias voltage across a PN junction is increased, the width of the depletion region will

1. Decrease
2. **Increase**
3. Stays the same
4. None of these
5. No way to determine

* The charge stored in the depletion region increases as the reverse bias voltage increases, which causes a capacitance.

**TRUE**

* Which of the following is true for a semiconductor doped P-type at 300°K ?

1. **The number of holes is greater than the number of free electrons**
2. The number of holes is equal to the number of free electrons
3. Both the number of holes and the number of free electrons are equal to zero
4. None of these
5. The number of holes is less than the number of free electrons

* If a semiconductor is doped with acceptor atoms, then:

1. There are the same number of free electrons and holes
2. **There are many more holes than free electrons**
3. None of these
4. There could be either more holes, or more free electrons
5. There are many more free electrons than holes

* When p-type silicon is brought into contact with n-type silicon, a PN junction is formed.

**TRUE**

* The ionized atoms in the depletion region cause a separation of charge between the two sides of a PN junction, with positive charge on the p-side and negative charge on the n-side.

**FALSE**

* Boron (B) is commonly used as a donor atom in silicon.

**FALSE**

* As the forward bias voltage across a PN junction is decreased, the potential barrier will

1. None of these
2. Decrease
3. Stays the same
4. **Increase**
5. No way to determine

* When the donor and acceptor atoms near a PN junction are ionized, this uncovers bound charge which cannot move.

**TRUE**

* As the forward bias across a PN junction is decreased, the potential barrier increases.

**TRUE**

* The Avalanche effect typically causes the reverse breakdown of PN junctions which break down at voltages < 5V.

**FALSE**

* As the forward bias across a PN junction is increased, the width of the depletion region increases.

**FALSE**

* As the reverse bias voltage across a PN junction is increased, the potential barrier will

1. Stays the same
2. **Increase**
3. None of these
4. Decrease
5. No way to determine

* The depletion region surrounding a PN junction contains almost no immobile ions.

**FALSE**

* At room temperature (300°K) there is enough thermal energy to break some bonds and create electron-hole pairs.

**TRUE**

* The diffusion capacitance for a PN junction is directly proportional to the average time it takes for a carrier to recombine after it crosses the junction.

**TRUE**

* Germanium is the most widely used semiconductor today.

**FALSE**

* When p-type silicon is brought into contact with n-type silicon, holes diffuse from the N side to the P side, and electrons diffuse from the P side to the N side.

**FALSE**

* When a free electron moves away from it’s donor atom, it leaves behind a negatively charged ion.

**FALSE**

* As the forward bias voltage across a PN junction is increased, the width of the depletion region will

1. Increase
2. No way to determine
3. None of these
4. Stays the same
5. **Decrease**

* As the temperature of a PN junction increases, the “built-in voltage” varies due to changes in both the thermal voltage, kT/q, and the intrinsic carrier concentration, ni.

**TRUE**

* Which of the following is true for a semiconductor doped N-type at 300°K ?

1. **The number of holes is less than the number of free electrons**
2. The number of holes is greater than the number of free electrons
3. The number of holes is equal to the number of free electrons
4. All of these
5. Both the number of holes and the number of free electrons are equal to zero

* Both electrons and holes are charge carriers which can move around and conduct electricity.

**TRUE**

* Heavily doped PN junctions break down at lower reverse voltages than lightly doped PN junctions.

**TRUE**

* When silicon is doped with donor atoms, this increases the number of electrons.

**TRUE**

* Doped semiconductors are pure, without any impurity atoms added.

**FALSE**

* The depletion region capacitance increases nonlinearly as the reverse bias voltage is decreased.

**TRUE**

* A hole is really just the absence of an electron, and can be thought of as a negatively charged particle.

**FALSE**

* The ionized atoms in the depletion region cause a separation of charge between the two sides of a PN junction, with positive charge on the n-side and negative charge on the p-side.

**TRUE**

* As the reverse bias across a PN junction is decreased, the width of the depletion region increases.

**FALSE**

* Boron (B) is commonly used as an acceptor atom in silicon.

**TRUE**

* As the reverse bias voltage across a PN junction is decreased, the width of the depletion region will

1. Stays the same
2. None of these
3. **Decrease**
4. Increase
5. No way to determine

* As the forward bias across a PN junction is decreased, the width of the depletion region decreases.

**FALSE**

* As the forward bias across a PN junction is decreased, the width of the depletion region increases.

**TRUE**

* For abrupt step PN junctions, the depletion capacitance depends on the square root of the reverse bias voltage.

**TRUE**

* A hole is really just the absence of an electron, and can be thought of as a positively charged particle.

**TRUE**

* The p-side of a PN junction is called the anode, and the n-side of the PN junction is called the cathode.

**TRUE**

* When a hole moves away from it’s acceptor atom, it leaves behind a positively charged ion.

**FALSE**

* As the reverse bias voltage across a PN junction is decreased, the depletion capacitance will

1. Decrease
2. Stays the same
3. None of these
4. No way to determine
5. **Increase**

* Both electrons and holes are charge carriers which can form covalent bonds between atoms.

**FALSE**

* In a semiconductor the number of holes multiplied by the number of electrons is equal to a constant except when dopant atoms are added.

**FALSE**

* When silicon is doped with donor atoms, this increases the number of holes.

**FALSE**

* The diffusion capacitance for a PN junction is inversely proportional to the DC bias current for the junction.

**FALSE**

* Both holes and electrons leave behind immobile ions when they conduct electricity.

**TRUE**

* The separation of charge caused by the immobile ions in the depletion region surrounding a PN junction creates an electric field, which opposes the further diffusion of electrons and holes.

**TRUE**

* As the reverse bias across a PN junction is decreased, the potential barrier decreases.

**TRUE**

* Acceptor atoms have 5 electrons in their outer most shell.

**FALSE**

* For linearly graded PN junctions, the depletion capacitance depends on the square root of the reverse bias voltage.

**FALSE**

* In a semiconductor doped with acceptor atoms, the number of electrons is much higher than the number of holes.

**FALSE**

* The minimum value for the depletion region capacitance of a reverse biased PN junction occurs when the reverse bias is equal to zero volts.

**FALSE**

* When silicon is doped with acceptor atoms, this increases the number of electrons.

**FALSE**

* The diffusion capacitance for a PN junction models the variations in the excess charge stored as carriers are injected across the junction with variations in the reverse bias voltage applied.

**FALSE**

* The Zener effect typically causes the reverse breakdown of PN junctions which break down at voltages < 5V.

**TRUE**

* The separation of charge caused by the immobile ions in the depletion region surrounding a PN junction causes the “built-in voltage”, which opposes the further diffusion of electrons and holes.

**TRUE**

* As the reverse bias across a PN junction is increased, the potential barrier decreases.

**FALSE**

* As the reverse bias across a PN junction is increased, the potential barrier increases.

TRUE

* As the forward bias across a PN junction is increased, the potential barrier decreases.

**TRUE**

* As the forward bias across a PN junction is increased, the potential barrier increases.

**FALSE**

* As the temperature of a PN junction increases, the “built-in voltage” increases directly proportional to changes in the thermal voltage, kT/q.

**FALSE**

* As the forward bias across a PN junction is increased, the width of the depletion region decreases.

**TRUE**

* As the reverse bias across a PN junction is increased, the width of the depletion region increases.

**TRUE**

* When the donor and acceptor atoms near a PN junction are ionized, the ionized atoms move away from the junction.

**FALSE**

* The Zener effect typically causes the reverse breakdown of PN junctions which break down at voltages > 7V.

**FALSE**

* The depletion region capacitance decreases nonlinearly as the reverse bias voltage is increased.

**TRUE**

* As the reverse bias across a PN junction is decreased, the width of the depletion region decreases.

**TRUE**

* The reverse breakdown voltage of a PN junction decreases as the doping levels increase.

**TRUE**

* Lightly doped PN junctions break down at lower reverse voltages than heavily doped PN junctions.

**FALSE**

* The diffusion capacitance for a PN junction is directly proportional to the DC bias current for the junction.

**TRUE**

# PRACTICE QUIZ 04

* In a Half-wave rectifier with a filter capacitor, the minimum breakdown voltage required for the diodes is :

1. None of these
2. The peak input voltage minus 1 diode drop
3. The peak-to-peak input voltage
4. **The peak-to-peak input voltage minus 1 diode drop**
5. The peak input voltage

* A Full Wave Rectifier allows only the positive or negative peaks of the input sine wave through to the output, but not both.

**FALSE**

* Which of the following is true for the small-signal resistance of a forward biased diode?

1. **All of these**
2. The small-signal resistance of a diode increases as the temperature increases
3. The small-signal resistance of a diode does NOT model the resistance of the silicon used to build the diode
4. The small-signal resistance of a diode decreases as the bias current increases
5. The small-signal resistance of a diode can be measured from the slope of the diode I-V curve

* Which of the following is true for the small-signal resistance of a forward biased diode?

1. The small-signal resistance of a diode is equal to the slope of the diode I-V curve
2. The small-signal resistance of a diode models the resistance of the silicon used to build the diode
3. **The small-signal resistance of a diode increases as the temperature increases**
4. None of these
5. The small-signal resistance of a diode increases as the bias current increases

* Which of the following is true for the small-signal resistance of a forward biased diode?

1. The small-signal resistance of a diode decreases as the temperature increases
2. The small-signal resistance of a diode increases as the bias current increases
3. All of these
4. The small-signal resistance of a diode is equal to the slope of the diode I-V curve
5. **The small-signal resistance of a diode does NOT model the resistance of the silicon used to build the diode**

* Which of the following is true for the small-signal resistance of a forward biased diode?

1. The small-signal resistance of a diode decreases as the temperature increases
2. The small-signal resistance of a diode is equal to the slope of the diode I-V curve
3. The small-signal resistance of a diode models the resistance of the silicon used to build the diode
4. All of these
5. **The small-signal resistance of a diode decreases as the bias current increases**

* Which of the following is true for the small-signal resistance of a forward biased diode?

1. The small-signal resistance of a diode decreases as the temperature increases
2. **The small-signal resistance of a diode can be measured from the slope of the diode I-V curve**
3. The small-signal resistance of a diode increases as the bias current increases
4. The small-signal resistance of a diode models the resistance of the silicon used to build the diode
5. None of these

* Which of the following is true for the small-signal resistance of a forward biased diode?

1. The small-signal resistance of a diode models the resistance of the silicon used to build the diode
2. The small-signal resistance of a diode increases as the bias current increases
3. The small-signal resistance of a diode is equal to the slope of the diode I-V curve
4. The small-signal resistance of a diode decreases as the temperature increases
5. **None of these**

* The RC time constant for the filter capacitor in a power supply is typically set so large that the capacitor discharge appears linear.

**TRUE**

* Which of the following would cause the ripple voltage at the output of a power supply to increase?

1. Reducing the size of the filter capacitor
2. Increasing the amplitude of the input voltage
3. Reducing the frequency of the input voltage
4. Reducing the size of the load resistance
5. **All of these**

* Which of the following would cause the ripple voltage at the output of a power supply to increase?

1. Increasing the size of the load resistance
2. All of these
3. **Reducing the frequency of the input voltage**
4. Reducing the amplitude of the input voltage
5. Increasing the size of the filter capacitor

* Which of the following would cause the ripple voltage at the output of a power supply to increase?

1. **Increasing the amplitude of the input voltage**
2. Increasing the frequency of the input voltage
3. Increasing the size of the filter capacitor
4. Increasing the size of the load resistance
5. None of these

* Which of the following would cause the ripple voltage at the output of a power supply to increase?

1. **Reducing the size of the filter capacitor**
2. Increasing the size of the load resistance
3. None of these
4. Reducing the amplitude of the input voltage
5. Increasing the frequency of the input voltage

* Which of the following would cause the ripple voltage at the output of a power supply to increase?

1. Reducing the amplitude of the input voltage
2. Increasing the frequency of the input voltage
3. All of these
4. Increasing the size of the filter capacitor
5. **Reducing the size of the load resistance**

* Which of the following would cause the ripple voltage at the output of a power supply to increase?

1. **None of these**
2. Increasing the size of the load resistance
3. Increasing the size of the filter capacitor
4. Increasing the frequency of the input voltage
5. Reducing the amplitude of the input voltage

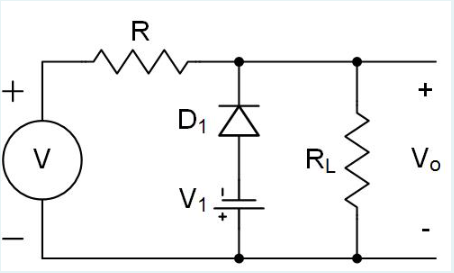
* When performing a Load Line analysis on a diode circuit to find the bias point, the operating point for the diode is where the linear equation for the circuit crosses the diode’s nonlinear I-V characteristic curve.

**TRUE**

* In the small-signal equivalent for a circuit containing a reverse biased Zener diode, the diode is replaced by it’s small-signal model which is a DC battery.

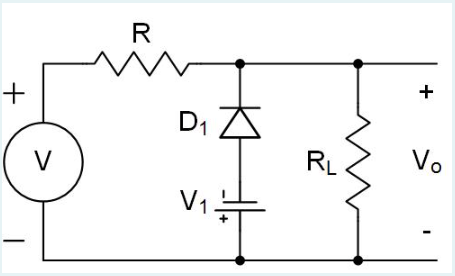
**FALSE**

* Assuming ideal diodes, for the diode circuit shown :



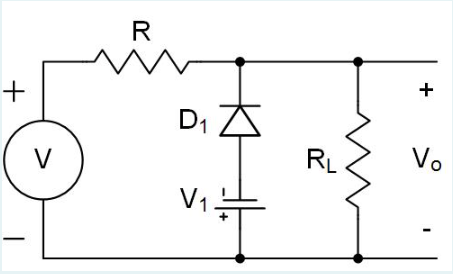
1. The gain is equal to RL/(R+RL) when V is > -V1
2. **All of these**
3. The minimum output voltage is -V1
4. The maximum output voltage is not limited
5. The gain is equal to 0 when V is < -V1

* Assuming ideal diodes, for the diode circuit shown :



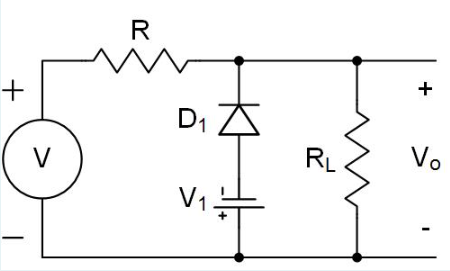
1. All of these
2. The minimum output voltage is +V1
3. **The gain is equal to RL/(R+RL) when V is > -V1**
4. The maximum output voltage is +V1
5. The gain is equal to RL/(R+RL) when V is < -V1

* Assuming ideal diodes, for the diode circuit shown :



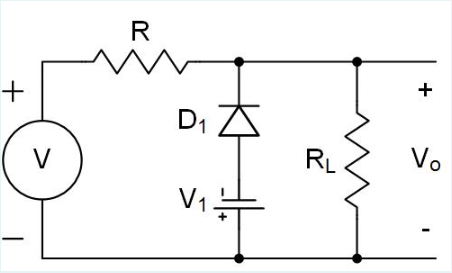
1. The gain is equal to RL/(R+RL) when V is < -V1
2. **The minimum output voltage is -V1**
3. None of these
4. The gain is equal to 0 when V is > -V1
5. The maximum output voltage is +V1

* Assuming ideal diodes, for the diode circuit shown :



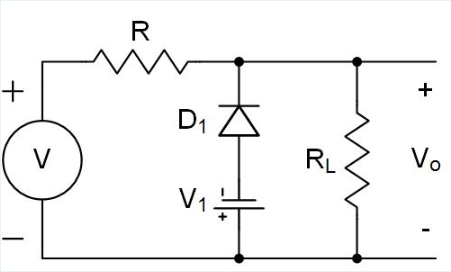
1. **The gain is equal to 0 when V is < -V1**
2. The gain is equal to 0 when V is > -V1
3. The minimum output voltage is +V1
4. The maximum output voltage is +V1
5. None of these

* Assuming ideal diodes, for the diode circuit shown :



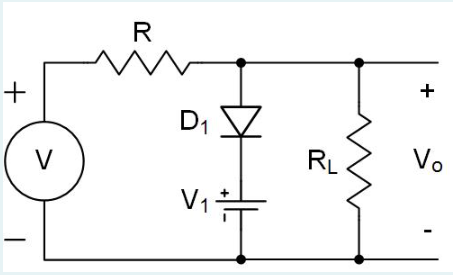
1. The gain is equal to 0 when V is > -V1
2. **The maximum output voltage is not limited**
3. All of these
4. The minimum output voltage is +V1
5. The gain is equal to RL/(R+RL) when V is < -V1

* Assuming ideal diodes, for the diode circuit shown :



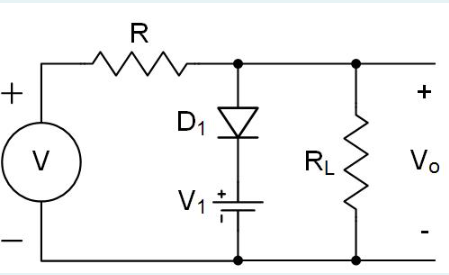
1. The gain is equal to RL/(R+RL) when V is < -V1
2. The maximum output voltage is +V1
3. The gain is equal to 0 when V is > -V1
4. **None of these**
5. The minimum output voltage is +V1

* Assuming ideal diodes, for the diode circuit shown :



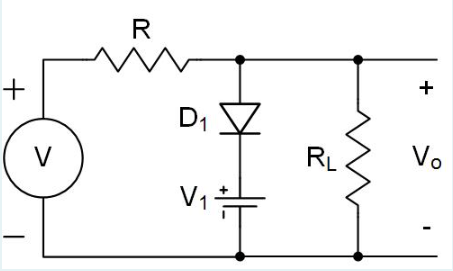
1. The gain is equal to RL/(R+RL) when V is < +V1
2. The maximum output voltage is +V1
3. The gain is equal to 0 when V is > +V1
4. **All of these**
5. The minimum output voltage is not limited

* Assuming ideal diodes, for the diode circuit shown :



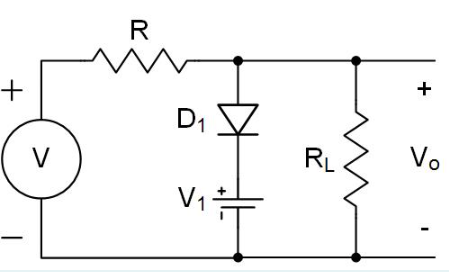
1. **The gain is equal to 0 when V is > +V1**
2. The minimum output voltage is +V1
3. None of these
4. The maximum output voltage is -V1
5. The gain is equal to 0 when V is < +V1

* Assuming ideal diodes, for the diode circuit shown :



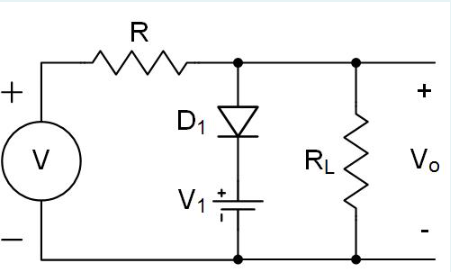
1. The maximum output voltage is -V1
2. The gain is equal to RL/(R+RL) when V is > +V1
3. The gain is equal to 0 when V is < +V1
4. All of these
5. **The minimum output voltage is not limited**

* Assuming ideal diodes, for the diode circuit shown :



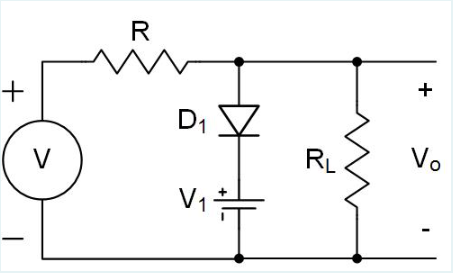
1. The minimum output voltage is +V1
2. The gain is equal to 0 when V is < +V1
3. None of these
4. **The maximum output voltage is +V1**
5. The gain is equal to RL/(R+RL) when V is > +V1

* Assuming ideal diodes, for the diode circuit shown :



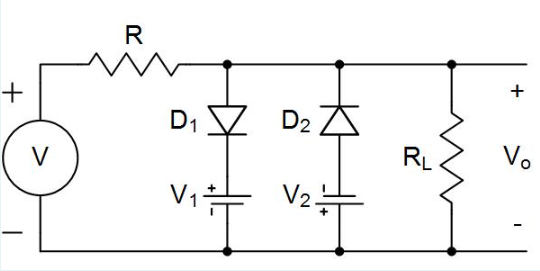
1. All of these
2. The maximum output voltage is -V1
3. **The gain is equal to RL/(R+RL) when V is < +V1**
4. The gain is equal to RL/(R+RL) when V is > +V1
5. The minimum output voltage is +V1

* Assuming ideal diodes, for the diode circuit shown :



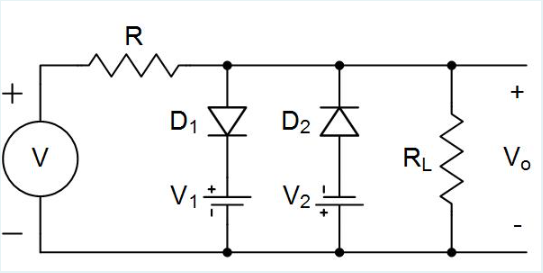
1. The gain is equal to RL/(R+RL) when V is > +V1
2. **None of these**
3. The maximum output voltage is -V1
4. The gain is equal to 0 when V is < +V1
5. The minimum output voltage is +V1

* Assuming ideal diodes, for the diode circuit shown :



1. The maximum output voltage is +V1
2. The gain is equal to RL/(R+RL) when V is < +V1 and > -V2
3. The minimum output voltage is -V2
4. The gain is equal to 0 when V is > +V1, or < -V2
5. **All of these**

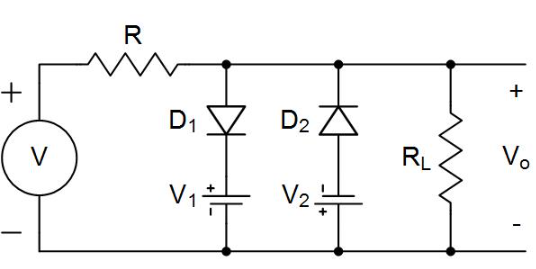
* Assuming ideal diodes, for the diode circuit shown :



1. The gain is equal to 0 when V is < +V1 and > -V2
2. None of these
3. The maximum output voltage is -V1
4. **The gain is equal to 0 when V is > +V1, or < -V2**
5. The minimum output voltage is +V2

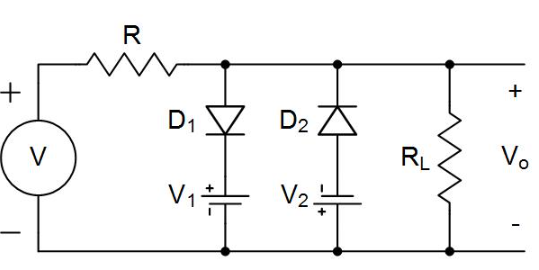
—-----------------------------------------------------------------------------------------

* Assuming ideal diodes, for the diode circuit shown :



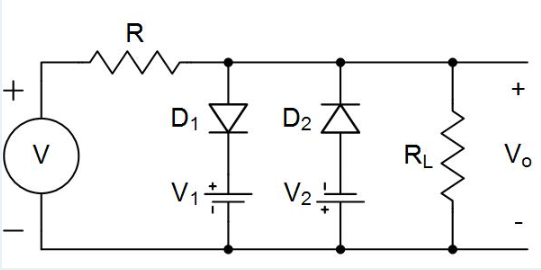
1. The minimum output voltage is +V2
2. The maximum output voltage is -V1
3. The gain is equal to RL/(R+RL) when V is > +V1, or < -V2
4. All of these
5. **The gain is equal to RL/(R+RL) when V is < +V1 and > -V2**

* Assuming ideal diodes, for the diode circuit shown :



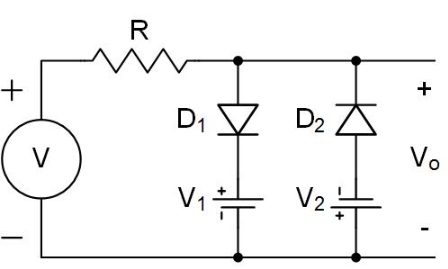
1. The gain is equal to 0 when V is < +V1 and > -V2
2. The gain is equal to RL/(R+RL) when V is > +V1, or < -V2
3. All of these
4. **The minimum output voltage is -V2**
5. The maximum output voltage is -V1

* Assuming ideal diodes, for the diode circuit shown :



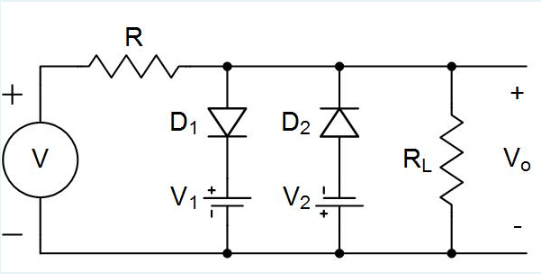
1. **The maximum output voltage is +V1**
2. None of these
3. The gain is equal to 0 when V is < +V1 and > -V2
4. The minimum output voltage is +V2
5. The gain is equal to RL/(R+RL) when V is > +V1, or < -V2

* Assuming ideal diodes, for the diode circuit shown :



1. All of these
2. **The minimum output voltage is -V2**
3. The gain is equal to 1 when V is > +V1, or < -V2
4. The gain is equal to 0 when V is < +V1 and > -V2
5. The maximum output voltage is -V1

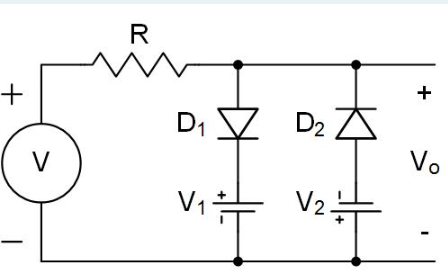
* Assuming ideal diodes, for the diode circuit shown :



1. The maximum output voltage is -V1
2. **None of these**
3. The gain is equal to 0 when V is < +V1 and > -V2
4. The gain is equal to RL/(R+RL) when V is > +V1, or < -V2
5. The minimum output voltage is +V2

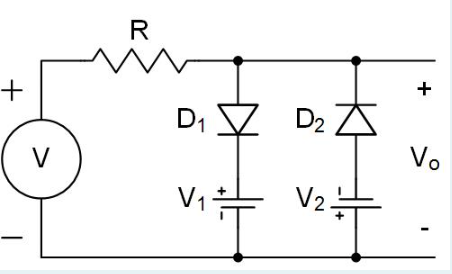
—---------------------------------------------------------------------------------------------------

* Assuming ideal diodes, for the diode circuit shown :



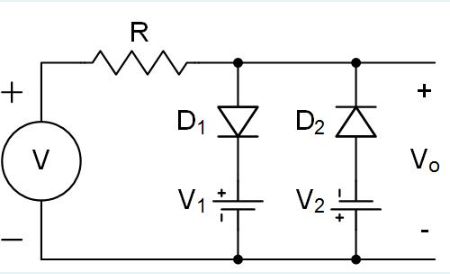
1. The maximum output voltage is +V1
2. The gain is equal to 0 when V is > +V1, or < -V2
3. **All of these**
4. The gain is equal to 1 when V is < +V1 and > -V2
5. The minimum output voltage is -V2

* Assuming ideal diodes, for the diode circuit shown :



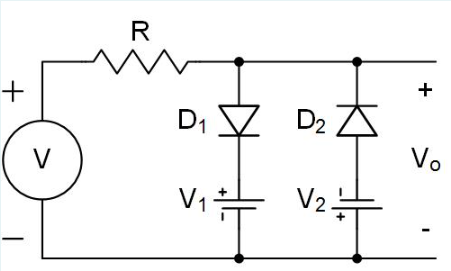
1. The maximum output voltage is -V1
2. The gain is equal to 0 when V is < +V1 and > -V2
3. The gain is equal to 1 when V is > +V1, or < -V2
4. The minimum output voltage is +V2
5. **None of these**

* Assuming ideal diodes, for the diode circuit shown :



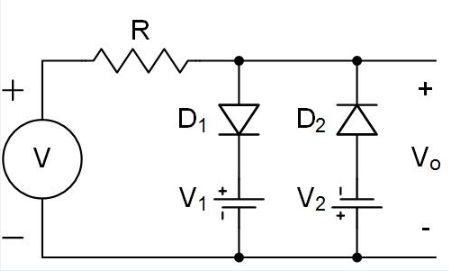
1. The maximum output voltage is -V1
2. The minimum output voltage is +V2
3. **The gain is equal to 1 when V is < +V1 and > -V2**
4. All of these
5. The gain is equal to 1 when V is > +V1, or < -V2

* Assuming ideal diodes, for the diode circuit shown :



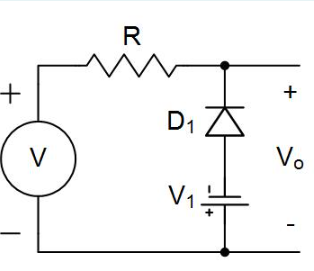
1. The gain is equal to 0 when V is < +V1 and > -V2
2. **The maximum output voltage is +V1**
3. The gain is equal to 1 when V is > +V1, or < -V2
4. The minimum output voltage is +V2
5. None of these

* Assuming ideal diodes, for the diode circuit shown :



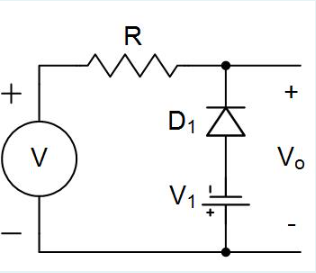
1. None of these
2. The maximum output voltage is -V1
3. The gain is equal to 0 when V is < +V1 and > -V2
4. **The gain is equal to 0 when V is > +V1, or < -V2**
5. The minimum output voltage is +V2

* Assuming ideal diodes, for the diode circuit shown :



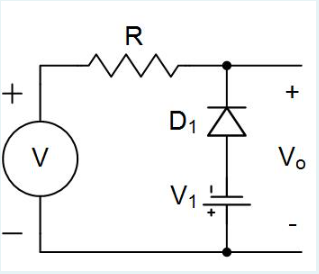
1. **All of these**
2. The maximum output voltage is not limited
3. The gain is equal to 0 when V is < -V1
4. The gain is equal to 1 when V is > -V1
5. The minimum output voltage is -V1

* Assuming ideal diodes, for the diode circuit shown :



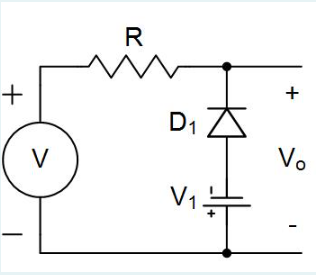
1. The gain is equal to 1 when V is < -V1
2. The minimum output voltage is +V1
3. **The gain is equal to 1 when V is > -V1**
4. All of these
5. The maximum output voltage is +V1

* Assuming ideal diodes, for the diode circuit shown :



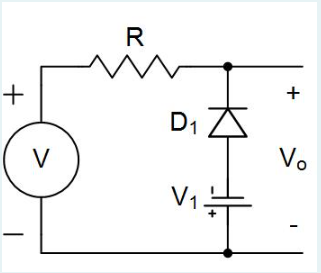
1. The maximum output voltage is +V1
2. **The gain is equal to 0 when V is < -V1**
3. The minimum output voltage is +V1
4. The gain is equal to 0 when V is > -V1
5. None of these

* Assuming ideal diodes, for the diode circuit shown :



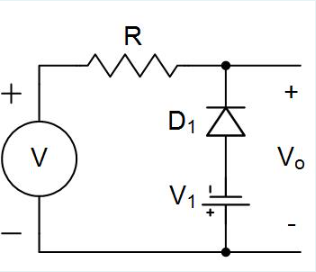
1. The maximum output voltage is +V1
2. None of these
3. The gain is equal to 0 when V is > -V1
4. The gain is equal to 1 when V is < -V1
5. **The minimum output voltage is -V1**

* Assuming ideal diodes, for the diode circuit shown :



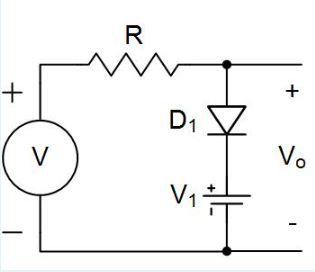
1. **The maximum output voltage is not limited**
2. The gain is equal to 0 when V is > -V1
3. The minimum output voltage is +V1
4. The gain is equal to 1 when V is < -V1
5. All of these

* Assuming ideal diodes, for the diode circuit shown :



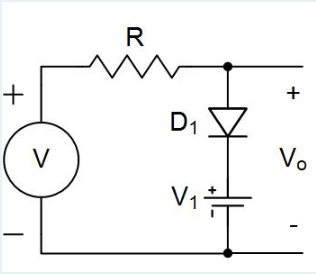
1. The maximum output voltage is +V1
2. The gain is equal to 0 when V is > -V1
3. **None of these**
4. The minimum output voltage is +V1
5. The gain is equal to 1 when V is < -V1

* Assuming ideal diodes, for the diode circuit shown :



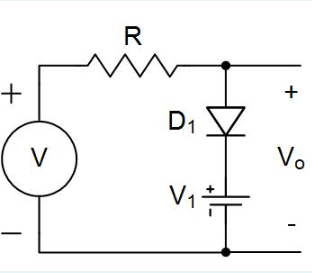
1. The minimum output voltage is not limited
2. The maximum output voltage is +V1
3. **All of these**
4. The gain is equal to 1 when V is < +V1
5. The gain is equal to 0 when V is > +V1

* Assuming ideal diodes, for the diode circuit shown :



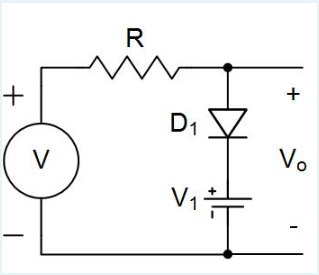
1. The gain is equal to 1 when V is > +V1
2. **The gain is equal to 1 when V is < +V1**
3. The minimum output voltage is +V1
4. The maximum output voltage is -V1
5. All of these

* Assuming ideal diodes, for the diode circuit shown :



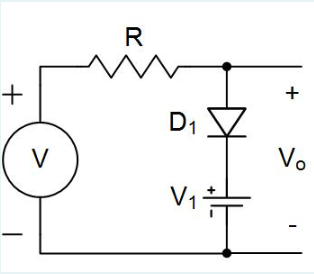
1. All of these
2. The gain is equal to 0 when V is < +V1
3. **The minimum output voltage is not limited**
4. The gain is equal to 1 when V is > +V1
5. The maximum output voltage is -V1

* Assuming ideal diodes, for the diode circuit shown :



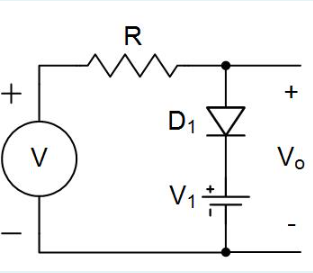
1. The maximum output voltage is -V1
2. **The gain is equal to 0 when V is > +V1**
3. The minimum output voltage is +V1
4. The gain is equal to 0 when V is < +V1
5. None of these

* Assuming ideal diodes, for the diode circuit shown :



1. The minimum output voltage is +V1
2. The gain is equal to 1 when V is > +V1
3. The gain is equal to 0 when V is < +V1
4. **The maximum output voltage is +V1**
5. None of these

* Assuming ideal diodes, for the diode circuit shown :



1. The minimum output voltage is +V1
2. The gain is equal to 0 when V is < +V1
3. The maximum output voltage is -V1
4. The gain is equal to 1 when V is > +V1
5. **None of these**

* One of the most useful applications for diodes is in DC power supplies, which convert a DC input voltage into an AC output voltage.

**FALSE**

* Which of the following is the best balance between ease of use and accuracy to quickly analyze diode circuits?

1. Graphical analysis using a load line
2. The ideal diode model
3. **The constant voltage drop diode model**
4. None of these
5. Iterative analysis using the exponential diode model

* Silicon diodes start to carry a significant amount of current once the forward bias voltage across the diode exceeds 0V at room temperature.

**FALSE**

* In the small-signal equivalent for a circuit containing a reverse biased Zener diode, the diode is replaced by it’s small-signal model which is a DC battery in series with the diode’s incremental resistance.

**TRUE**

* Which of the following is true about the small-signal model for a reverse biased diode?

1. The incremental resistance of the diode can be measured from the slope of the diode I-V curve
2. **All of these**
3. The reverse diode voltage equals the battery voltage plus the current times the incremental resistance
4. The small-signal model is valid for reverse bias voltages > the knee voltage, Vzk
5. The small-signal model is valid for reverse bias currents > the knee current, Izk

* Which of the following is true about the small-signal model for a reverse biased diode?

1. The incremental resistance of the diode is equal to the slope of the diode I-V curve
2. The small-signal model is valid for any amount of reverse bias current
3. None of these
4. The reverse diode voltage is equal to the battery voltage for all values of current
5. **The small-signal model is valid for reverse bias voltages > the knee voltage, Vzk**

* Which of the following is true about the small-signal model for a reverse biased diode?

1. None of these
2. The small-signal model is valid for any amount of reverse bias current
3. The incremental resistance of the diode is equal to the slope of the diode I-V curve
4. **The reverse diode voltage equals the battery voltage plus the current times the incremental resistance**
5. The small-signal model is valid for any amount of reverse bias voltage

* Which of the following is true about the small-signal model for a reverse biased diode?

1. The reverse diode voltage is equal to the battery voltage for all values of current
2. All of these
3. **The small-signal model is valid for reverse bias currents > the knee current, Izk**
4. The small-signal model is valid for any amount of reverse bias voltage
5. The incremental resistance of the diode is equal to the slope of the diode I-V curve

* Which of the following is true about the small-signal model for a reverse biased diode?

1. The small-signal model is valid for any amount of reverse bias current
2. All of these
3. The reverse diode voltage is equal to the battery voltage for all values of current
4. The small-signal model is valid for any amount of reverse bias voltage
5. **The incremental resistance of the diode can be measured from the slope of the diode I-V curve**

* Which of the following is true about the small-signal model for a reverse biased diode?

1. The small-signal model is valid for any amount of reverse bias voltage
2. **None of these**
3. The incremental resistance of the diode is equal to the slope of the diode I-V curve
4. The small-signal model is valid for any amount of reverse bias current
5. The reverse diode voltage is equal to the battery voltage for all values of current

* Which of these circuits requires the diodes used to have the highest peak inverse voltage rating?

1. Full-wave rectifiers using a bridge rectifier
2. Same for all of these
3. Impossible to determine
4. **Full-wave rectifiers using a center-tapped transformer**
5. Half-wave rectifiers without a filter capacitor

* A Voltage Doubler circuit can be built by combining a clamped capacitor circuit with a DC restorer circuit.

**FALSE**

* When is the current flowing through a diode approximately constant?

1. **When the voltage on the N side is higher than the voltage on the P side, but lower than the breakdown voltage**
2. None of these
3. When the voltage on the P side is higher than the voltage on the N side
4. When the voltage on the N side is higher than the voltage on the P side, and higher than the breakdown voltage
5. When the voltage on the P side is higher than the voltage on the N side by at least 500mV

* Peak Detectors are often used to charge up a capacitor to the average value of an input signal.

**FALSE**

* A Voltage Doubler circuit requires two diodes and two capacitors.

**TRUE**

* As the bias current flowing through a forward biased silicon diode at room temperature increases, the voltage across the diode will decrease at a rate of about -60mV per decade of current increase.

**FALSE**

* Which of the following circuits is part of a typical DC power supply?

1. **All of these**
2. A low pass filter
3. A voltage regulator
4. A power transformer
5. A diode rectifier

* Which of the following circuits is part of a typical DC power supply?

1. All of these
2. **A diode rectifier**
3. A current regulator
4. A high pass filter
5. A load resistor

* Which of the following circuits is part of a typical DC power supply?

1. A diode limiter
2. A load resistor
3. **None of these**
4. A high pass filter
5. A current regulator

* Which of the following circuits is part of a typical DC power supply?

1. A load resistor
2. A high pass filter
3. All of these
4. **A voltage regulator**
5. A diode limiter

* Which of the following circuits is part of a typical DC power supply?

1. None of these
2. A diode limiter
3. **A low pass filter**
4. A current regulator
5. A load resistor

* Which of the following circuits is part of a typical DC power supply?

1. **A power transformer**
2. None of these
3. A high pass filter
4. A diode limiter
5. A current regulator

* The RC time constant for the filter capacitor in a power supply is typically set much larger than the period of the input sine wave.

**TRUE**

* In a Peak Detector diode circuit, which of the following is true?

1. The charge supplied to the load is replaced by the diode each time the input voltage reaches it’s peak
2. The diode must have a breakdown voltage larger than the peak-to-peak input voltage
3. The output voltage is equal to the maximum input voltage
4. **All of these**
5. The diode turns on briefly in the beginning, but then is off most of the time

* In a Peak Detector diode circuit, which of the following is true?

1. The charge supplied to the load is replaced by the capacitor each time the input voltage reaches it’s peak
2. The output voltage is always equal to the input voltage
3. The diode must have a breakdown voltage equal to the peak input voltage
4. All of these
5. **The diode turns on briefly in the beginning, but then is off most of the time**

* In a Peak Detector diode circuit, which of the following is true?

1. All of these
2. The diode turns on briefly in the beginning, but then is on most of the time
3. The output voltage is always equal to the input voltage
4. The diode must have a breakdown voltage equal to the peak input voltage
5. **The charge supplied to the load is replaced by the diode each time the input voltage reaches it’s peak**

* In a Peak Detector diode circuit, which of the following is true?

1. **The output voltage is equal to the maximum input voltage**
2. None of these
3. The charge supplied to the load is replaced by the capacitor each time the input voltage reaches it’s peak
4. The diode turns on briefly in the beginning, but then is on most of the time
5. The diode must have a breakdown voltage equal to the peak input voltage

* In a Peak Detector diode circuit, which of the following is true?

1. **The diode must have a breakdown voltage equal to the peak-to-peak input voltage**
2. The diode turns on briefly in the beginning, but then is on most of the time
3. The charge supplied to the load is replaced by the capacitor each time the input voltage reaches it’s peak
4. None of these
5. The output voltage is always equal to the input voltage

* In a Peak Detector diode circuit, which of the following is true?

1. The diode must have a breakdown voltage equal to the peak input voltage
2. The diode turns on briefly in the beginning, but then is on most of the time
3. The output voltage is always equal to the input voltage
4. **None of these**
5. The charge supplied to the load is replaced by the capacitor each time the input voltage reaches it’s peak

* The Exponential diode model provides the best accuracy when analyzing diode circuits, but requires an graphical approach to solve the nonlinear equations involved.

**FALSE**

* If the reverse bias voltage applied across a diode gets too high and exceeds the breakdown voltage for the diode, then the forward current flowing through the diode will increase sharply.

**FALSE**

* Peak Detectors are often used to create an output voltage which is equal to the average value of an input signal.

**FALSE**

* When does the current flowing through a diode depend exponentially on the voltage applied across the diode?

1. All of these
2. **When the voltage on the P side is higher than the voltage on the N side**
3. When the voltage on the N side is higher than the voltage on the P side, and higher than the breakdown voltage
4. When the voltage on the N side is higher than the voltage on the P side, but lower than the breakdown voltage
5. When the voltage on the P side is higher than the voltage on the N side by at least 500mV

* As the bias current flowing through a forward biased silicon diode at room temperature increases, the voltage across the diode will increase at a rate of about 60mV per decade of current increase.

**TRUE**

* Which of the following is true for a zener diode used as a voltage reference?

1. The amount the reference voltage varies when the input supply voltage varies is called the line regulation
2. The amount the reference voltage varies when the load current varies is called the load regulation
3. Once a zener diode is operating in the reverse breakdown region, the voltage across it only varies slightly
4. **All of these**
5. The input supply voltage used must always be larger than the reverse breakdown voltage of the zener diode

* Which of the following is true for a zener diode used as a voltage reference?

1. **The amount the reference voltage varies when the load current varies is called the load regulation**
2. The amount the reference voltage varies when the input supply voltage varies is called the load regulation
3. Once a zener diode is operating in the reverse breakdown region, the voltage across it doesn’t vary
4. The input supply voltage used must never be larger than the reverse breakdown voltage of the zener diode
5. All of these

* Which of the following is true for a zener diode used as a voltage reference?

1. The input supply voltage used must never be larger than the reverse breakdown voltage of the zener diode
2. Once a zener diode is operating in the reverse breakdown region, the voltage across it doesn’t vary
3. None of these
4. The amount the reference voltage varies when the load current varies is called the line regulation
5. **The amount the reference voltage varies when the input supply voltage varies is called the line regulation**

* Which of the following is true for a zener diode used as a voltage reference?

1. None of these
2. The amount the reference voltage varies when the input supply voltage varies is called the load regulation
3. The amount the reference voltage varies when the load current varies is called the line regulation
4. Once a zener diode is operating in the reverse breakdown region, the voltage across it doesn’t vary
5. **The input supply voltage used must always be larger than the reverse breakdown voltage of the zener diode**

* Which of the following is true for a zener diode used as a voltage reference?

1. All of these
2. The amount the reference voltage varies when the input supply voltage varies is called the load regulation
3. **Once a zener diode is operating in the reverse breakdown region, the voltage across it only varies slightly**
4. The amount the reference voltage varies when the load current varies is called the line regulation
5. The input supply voltage used must never be larger than the reverse breakdown voltage of the zener diode

* Which of the following is true for a zener diode used as a voltage reference?

1. The amount the reference voltage varies when the load current varies is called the line regulation
2. The input supply voltage used must never be larger than the reverse breakdown voltage of the zener diode
3. The amount the reference voltage varies when the input supply voltage varies is called the load regulation
4. Once a zener diode is operating in the reverse breakdown region, the voltage across it doesn’t vary
5. **None of these**

* Line regulation is a measure of how much a reference voltage changes as the load current changes.

**FALSE**

* In order to avoid problems with thermal runaway, diodes are usually biased with a constant current instead of at a constant voltage.

**TRUE**

* To solve a nonlinear circuit equation by iteration, you should use logarithms instead of exponentials to aid in convergence.

**TRUE**

* When a forward bias current flows through a diode, the voltage across the diode will increase logarithmically as the current through the diode increases linearly.

**TRUE**

* The final stage in a power supply is a voltage regulator, which keeps the output voltage constant as both the input voltage and the load current vary.

**TRUE**

* The Exponential diode model provides a good compromise between accuracy and ease of use when analyzing diode circuits.

**FALSE**

* Diode limiters can be used to make a sine wave look more like a square wave, which is useful in communications circuits.

**TRUE**

* In a half-wave rectifier the diode turns on once during each period of the input sine wave to recharge the filter capacitor.

**TRUE**

* Superposition can be used to analyze nonlinear devices such as diodes as long as the variations around the bias point are large enough.

**FALSE**

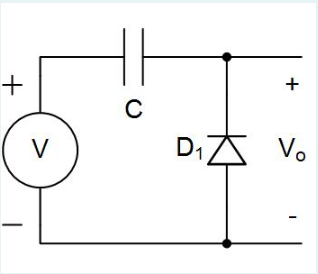
* For a Full Wave Rectifier the diodes must be able to handle a Peak Inverse Voltage equal to nearly the peak of the input voltage.

**FALSE**

* When does a diode “turn on” and start carrying a significant amount of current?

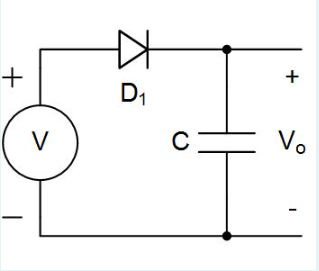
1. None of these
2. When the voltage on the N side is higher than the voltage on the P side, and higher than the breakdown voltage
3. **When the voltage on the P side is higher than the voltage on the N side by at least 500mV**
4. When the voltage on the P side is higher than the voltage on the N side
5. When the voltage on the N side is higher than the voltage on the P side, but lower than the breakdown voltage

* The diode circuit shown is a :



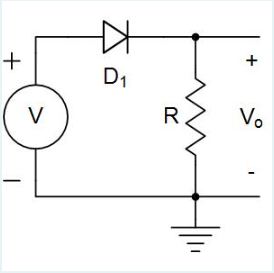
1. Peak detector circuit
2. Limiter circuit
3. **DC restorer circuit**
4. None of these
5. Voltage doubler circuit

* The diode circuit shown is a :



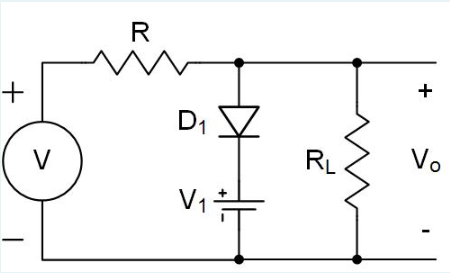
1. Limiter circuit
2. DC restorer circuit
3. Voltage doubler circuit
4. **Peak detector circuit**
5. None of these

* The diode circuit shown is a :



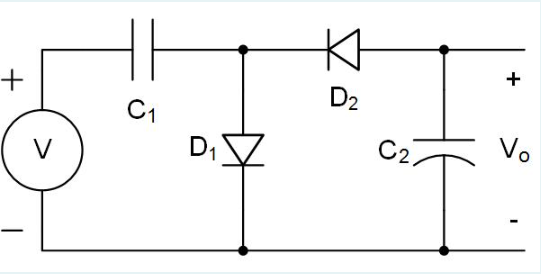
1. DC restorer circuit
2. Peak detector circuit
3. Voltage doubler circuit
4. **None of these**
5. Limiter circuit

* The diode circuit shown is a :



1. None of these
2. DC restorer circuit
3. Peak detector circuit
4. **Limiter circuit**
5. Voltage doubler circuit

* The diode circuit shown is a :



1. Limiter circuit
2. None of these
3. DC restorer circuit
4. Peak detector circuit
5. **Voltage doubler circuit**

* A Half Wave Rectifier allows only the positive or negative peaks of the input sine wave through to the output, but not both.

**TRUE**

* A Half Wave Rectifier allows both the positive and negative peaks of the input sine wave through to the output.

**FALSE**

* In a power supply a transformer is typically used to increase the low line voltage to a more useful, higher value.

**FALSE**

* Which of the following would NOT cause the ripple voltage at the output of a power supply to increase?

1. None of these
2. **Increasing the size of the load resistance**
3. Reducing the size of the filter capacitor
4. Reducing the frequency of the input voltage
5. Increasing the amplitude of the input voltage

* When a forward bias current flows through a diode, the voltage across the diode will increase exponentially as the current through the diode increases linearly.

**FALSE**

* In a DC Restorer diode circuit, which of the following is true?

1. The capacitor charges up to either the peak positive or peak negative input voltage, depending on the direction of the diode
2. The peak-to-peak output voltage is equal to the peak-to-peak input voltage
3. **All of these**
4. The average value of the output voltage is not equal to zero
5. The diode clamps one side of the capacitor to a fixed voltage, such as ground

* In a DC Restorer diode circuit, which of the following is true?

1. The peak-to-peak output voltage is equal to the peak input voltage
2. The average value of the output voltage is always equal to zero
3. The capacitor charges up to the average value of input voltage
4. All of these
5. **The diode clamps one side of the capacitor to a fixed voltage, such as ground**

* In a DC Restorer diode circuit, which of the following is true?

1. The peak-to-peak output voltage is equal to the peak input voltage
2. The capacitor clamps one side of the diode to a fixed voltage, such as ground
3. The average value of the output voltage is always equal to zero
4. **The capacitor charges up to either the peak positive or peak negative input voltage, depending on the direction of the diode**
5. None of these

* In a DC Restorer diode circuit, which of the following is true?

1. The capacitor charges up to the average value of input voltage
2. All of these
3. The capacitor clamps one side of the diode to a fixed voltage, such as ground
4. The peak-to-peak output voltage is equal to the peak input voltage
5. **The average value of the output voltage is not equal to zero**

* In a DC Restorer diode circuit, which of the following is true?

1. **The peak-to-peak output voltage is equal to the peak-to-peak input voltage**
2. The average value of the output voltage is always equal to zero
3. The capacitor charges up to the average value of input voltage
4. None of these
5. The capacitor clamps one side of the diode to a fixed voltage, such as ground

* In a DC Restorer diode circuit, which of the following is true?

1. The average value of the output voltage is always equal to zero
2. **None of these**
3. The peak-to-peak output voltage is equal to the peak input voltage
4. The capacitor clamps one side of the diode to a fixed voltage, such as ground
5. The capacitor charges up to the average value of input voltage

* For a Full Wave Rectifier the diodes must be able to handle a Peak Inverse Voltage equal to nearly twice the peak of the input voltage.

**TRUE**

* In Peak Detector circuits, the diodes conduct current the majority of the time.

**FALSE**

* Zener diodes are intentionally designed to operate in their reverse breakdown region so they can be used as voltage references.

**TRUE**

* A Voltage Doubler circuit requires two diodes and one capacitor.

**FALSE**

* Which of the of the following is true for a diode with a voltage Vd applied to the P side and the N side grounded?

1. **All of these**
2. The current through the diode, Id, grows linearly when Vd is decreased below the breakdown voltage
3. The diode “turns on” and starts carrying a significant amount of current when Vd is > 0.5V
4. The current through the diode, Id, is approximately constant when Vd is decreased slightly below 0V
5. The current through the diode, Id, grows exponentially when Vd is increased slightly above 0V

* Which of the of the following is true for a diode with a voltage Vd applied to the P side and the N side grounded?

1. None of these
2. **The current through the diode, Id, is approximately constant when Vd is decreased slightly below 0V**
3. The diode “turns on” and starts carrying a significant amount of current when Vd is < -0.5V
4. The current through the diode, Id, grows linearly when Vd is increased slightly above 0V
5. The current through the diode, Id, grows exponentially when Vd is decreased below the breakdown voltage

* Which of the of the following is true for a diode with a voltage Vd applied to the P side and the N side grounded?

1. The current through the diode, Id, grows exponentially when Vd is decreased slightly below 0V
2. The current through the diode, Id, grows linearly when Vd is increased slightly above 0V
3. **The diode “turns on” and starts carrying a significant amount of current when Vd is > 0.5V**
4. The current through the diode, Id, is approximately constant when Vd is decreased below the breakdown voltage
5. None of these

* Which of the of the following is true for a diode with a voltage Vd applied to the P side and the N side grounded?

1. **The current through the diode, Id, grows linearly when Vd is decreased below the breakdown voltage**
2. The diode “turns on” and starts carrying a significant amount of current when Vd is < -0.5V
3. The current through the diode, Id, grows linearly when Vd is increased slightly above 0V
4. The current through the diode, Id, grows exponentially when Vd is decreased slightly below 0V
5. All of these

* Which of the of the following is true for a diode with a voltage Vd applied to the P side and the N side grounded?

1. **The current through the diode, Id, grows exponentially when Vd is increased slightly above 0V**
2. The current through the diode, Id, is approximately constant when Vd is decreased below the breakdown voltage
3. All of these
4. The diode “turns on” and starts carrying a significant amount of current when Vd is < -0.5V
5. The current through the diode, Id, grows exponentially when Vd is decreased slightly below 0V

* Which of the of the following is true for a diode with a voltage Vd applied to the P side and the N side grounded?

1. **None of these**
2. The current through the diode, Id, grows linearly when Vd is increased slightly above 0V
3. The current through the diode, Id, grows exponentially when Vd is decreased slightly below 0V
4. The diode “turns on” and starts carrying a significant amount of current when Vd is < -0.5V
5. The current through the diode, Id, is approximately constant when Vd is decreased below the breakdown voltage

* The output voltage of a Voltage Doubler circuit is about twice the DC value of the input voltage.

**FALSE**

* Diode limiters are used to control the gain of a circuit before the diodes turn on.

**FALSE**

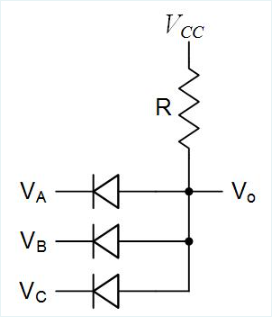
* In the small-signal equivalent for a circuit containing a forward biased diode, the diode is replaced by it’s small-signal resistance which is proportional to the operating temperature.

**TRUE**

* The peak current which flows in the rectifier diodes for a power supply is typically about twice the average current which flows in these same rectifier diodes.

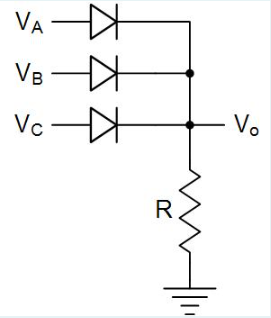
**TRUE**

* The digital logic circuit shown is a simple :



1. NOR gate
2. None of these
3. OR gate
4. **AND gate**
5. NAND gate

* The digital logic circuit shown is a simple :



1. None of these
2. NOR gate
3. **OR gate**
4. AND gate
5. NAND gate

* As temperature increases the voltage across a forward biased silicon diode will decrease.

**TRUE**

* In a power supply diodes are typically used to rectify the AC input voltage, which means converting a bipolar sine wave into a series of unipolar pulses.

**TRUE**

* A Load Line analysis is a graphical solution method which allows a nonlinear set of simultaneous equations to be solved, by plotting the linear equation for the circuit on the same plot with the diode’s nonlinear I-V characteristic curve.

**TRUE**

* Zener diodes are intentionally designed to operate in their reverse breakdown region so they can be used as current references.

**FALSE**

* In a rectifier the diodes only turn on for a short conduction interval every cycle to replace the charge which the filter capacitor supplied to the load while the diodes were turned off.

**TRUE**

* In a full-wave rectifier the diodes turn on once during each period of the input sine wave to recharge the filter capacitor.

**FALSE**

* The size of the ripple voltage at the output of a power supply filter capacitor is inversely proportional to the period of the input sine wave.

**FALSE**

* A small enough piece of anything nonlinear looks linear.

**TRUE**

* To solve a nonlinear circuit equation by iteration, you should use exponentials instead of logarithms to aid in convergence.

**FALSE**

* In Peak Detector circuits, the diodes don’t conduct current the majority of the time.

**TRUE**

* When does the current flowing through a diode depend linearly on the voltage applied across the diode?

1. When the voltage on the N side is higher than the voltage on the P side, but lower than the breakdown voltage
2. When the voltage on the P side is higher than the voltage on the N side by at least 500mV
3. All of these
4. When the voltage on the P side is higher than the voltage on the N side
5. **When the voltage on the N side is higher than the voltage on the P side, and higher than the breakdown voltage**

* The filter capacitor must be twice as large in a half-wave rectifier than in a full-wave rectifier to obtain the same ripple voltage.

**TRUE**

* Silicon diodes start to carry a significant amount of current once the forward bias voltage across the diode exceeds about 500mV at room temperature.

**TRUE**

* A Load Line analysis is a graphical solution method which allows a nonlinear set of simultaneous equations to be solved, by plotting the nonlinear equation for the circuit on the same plot with the diode’s linear I-V characteristic curve.

**FALSE**

* When does the voltage across a diode depend exponentially on the current flowing through?

1. When the voltage on the N side is higher than the voltage on the P side, and higher than the breakdown voltage
2. When the voltage on the P side is higher than the voltage on the N side by at least 500mV
3. When the voltage on the N side is higher than the voltage on the P side, but lower than the breakdown voltage
4. When the voltage on the P side is higher than the voltage on the N side
5. **None of these**

* The incremental resistance for a Zener diode is used to model how much the voltage across the reverse biased diode increases as the reverse current flowing through it increases.

**TRUE**

* The voltage across a forward biased silicon diode will change by about -2mV/°C as temperature changes.

**TRUE**

* A Voltage Doubler circuit can be built by combining a clamped capacitor circuit with a peak detector circuit.

**TRUE**

* The RC time constant for the filter capacitor in a power supply is typically set much smaller than the period of the input sine wave.

**FALSE**

* The output voltage for a bridge rectifier is just slightly lower than the output voltage for a full wave rectifier which uses a center-tapped transformer.

**TRUE**

* The output voltage for a bridge rectifier is just slightly higher than the output voltage for a full wave rectifier which uses a center-tapped transformer.

**FALSE**

* The filter capacitor used to filter the output pulses from a diode rectifier in a power supply is typically quite large, often bigger than 10F.

**FALSE**

* The RC time constant for the filter capacitor in a power supply is typically set so large that the capacitor discharge appears exponential.

**FALSE**

* In a DC Restorer circuit, a capacitor forces a diode to charge up to either the positive or negative peak of the input signal.

**FALSE**

* Peak Detectors are often used to charge up a capacitor to the maximum value of an input signal.

**TRUE**

* If the reverse bias voltage applied across a diode gets too high and exceeds the breakdown voltage for the diode, then the reverse current flowing through the diode will increase sharply.

**TRUE**

* At absolute zero (0°K) there is still enough thermal energy to break some bonds and create electron-hole pairs.

**FALSE**

* A bridge rectifier requires twice as many diodes as a full wave rectifier which uses a center-tapped transformer.

**TRUE**

* In the small-signal equivalent for a circuit containing a reverse biased Zener diode, the DC battery is used to model the diode’s reverse breakdown voltage at high current levels.

**FALSE**

* The filter capacitor used to filter the output pulses from a diode rectifier in a power supply is typically quite large, often bigger than 10μF.

**TRUE**

* As temperature increases the voltage across a forward biased silicon diode will increase.

**FALSE**

* In a full-wave rectifier the diodes turn on twice during each period of the input sine wave to recharge the filter capacitor.

**TRUE**

* Linear circuit analysis techniques can be applied to nonlinear circuits as long as the variations around the bias point are kept large enough.

**FALSE**

* As the bias current flowing through a forward biased silicon diode increases, the voltage across the diode will only increase slowly.

**TRUE**

* The peak current which flows in the rectifier diodes for a power supply is often much larger than the current supplied to the load.

**TRUE**

* The incremental resistance for a Zener diode is the slope of the diode’s I-V characteristic curve as the reverse voltage across the diode increases above the diode’s reverse breakdown voltage.

**FALSE**

* Bridge rectifiers are often used in power supplies instead of center-tapped transformers to lower cost.

**TRUE**

* The size of the ripple voltage at the output of a power supply filter capacitor is inversely proportional to the size of the filter capacitor used.

**TRUE**

* As the bias current flowing through a forward biased silicon diode increases, the voltage across the diode will increase quickly.

**FALSE**

* In a Voltage Doubler diode circuit, which of the following is true?

1. **All of these**
2. One of the diodes and one of the capacitors implement a clamped capacitor circuit
3. The output will be a DC voltage equal to either +2 or -2 times the peak input voltage, depending on the direction of the diodes
4. One of the diodes and one of the capacitors implement a peak detector circuit
5. The diodes must have a breakdown voltage larger than the peak-to-peak input voltage

* In a Voltage Doubler diode circuit, which of the following is true

1. **One of the diodes and one of the capacitors implement a peak detector circuit**
2. One of the diodes and one of the capacitors implement a rectifier circuit
3. The diodes must have a breakdown voltage equal to the peak input voltage
4. None of these
5. The output will be a sine wave with a peak of either +2 or -2 times the peak input voltage, depending on the direction of the diodes

* In a Voltage Doubler diode circuit, which of the following is true?

1. The output will be a sine wave with a peak of either +2 or -2 times the peak input voltage, depending on the direction of the diodes
2. One of the diodes and one of the capacitors implement a limiter circuit
3. One of the diodes and one of the capacitors implement a rectifier circuit
4. **The diodes must have a breakdown voltage larger than the peak-to-peak input voltage**
5. All of these

* In a Voltage Doubler diode circuit, which of the following is true?

1. **One of the diodes and one of the capacitors implement a clamped capacitor circuit**
2. The output will be a sine wave with a peak of either +2 or -2 times the peak input voltage, depending on the direction of the diodes
3. All of these
4. One of the diodes and one of the capacitors implement a limiter circuit
5. The diodes must have a breakdown voltage equal to the peak input voltage

* In a Voltage Doubler diode circuit, which of the following is true?

1. One of the diodes and one of the capacitors implement a limiter circuit
2. One of the diodes and one of the capacitors implement a rectifier circuit
3. The diodes must have a breakdown voltage equal to the peak input voltage
4. **The output will be a DC voltage equal to either +2 or -2 times the peak input voltage, depending on the direction of the diodes**
5. None of these

* In a Voltage Doubler diode circuit, which of the following is true?

1. The diodes must have a breakdown voltage equal to the peak input voltage
2. One of the diodes and one of the capacitors implement a rectifier circuit
3. **None of these**
4. One of the diodes and one of the capacitors implement a limiter circuit
5. The output will be a sine wave with a peak of either +2 or -2 times the peak input voltage, depending on the direction of the diodes

* A bridge rectifier requires half as many diodes as a full wave rectifier which uses a center-tapped transformer.

**FALSE**

* Peak Detectors are often used to create an output voltage which is equal to the maximum value of an input signal.

**TRUE**

* When a forward bias voltage is applied across a diode, the diode current will increase exponentially as the voltage across the diode increases linearly.

**TRUE**

* The simplest model to use when analyzing diode circuits is the Ideal Diode model, which assumes that the diode is a short circuit when forward biased and an open circuit when reverse biased.

**TRUE**

* The simplest model to use when analyzing diode circuits is the Ideal Diode model, which assumes that the diode is a 0.7V battery when forward biased and an open circuit when reverse biased.

**FALSE**

* In a rectifier the diodes only turn off for a short conduction interval every cycle to replace the charge which the filter capacitor supplied to the load while the diodes were turned on.

**FALSE**

* When a forward bias voltage is applied across a diode, the diode current will increase logarithmically as the voltage across the diode increases linearly.

**FALSE**

* In the small-signal equivalent for a circuit containing a forward biased diode, the diode is replaced by it’s small-signal resistance which is inversely proportional to the bias current.

**TRUE**

* Which of the following allows diode circuits to be analyzed without solving equations?

1. **Graphical analysis using a load line**
2. Iterative analysis using the exponential diode model
3. The ideal diode model
4. None of these
5. The constant voltage drop diode model

* The final stage in a power supply is a voltage regulator, which keeps the output voltage constant even if the output is shorted.

**FALSE**

* Which of the following allows diode circuits to be analyzed without using any equations or plots?

1. The ideal diode model
2. **None of these**
3. Iterative analysis using the exponential diode model
4. Graphical analysis using a load line
5. The constant voltage drop diode model

* In the small-signal equivalent for a circuit containing a forward biased diode, the diode is replaced by it’s small-signal resistance which is inversely proportional to the operating temperature.

**FALSE**

* The size of the ripple voltage at the output of a power supply filter capacitor is directly proportional to the size of the current supplied to the load.

**TRUE**

* In a half-wave rectifier the diode turns on twice during each period of the input sine wave to recharge the filter capacitor.

**FALSE**

* Which of the following will give the most accurate results when analyzing diode circuits?

1. The constant voltage drop diode model
2. **Iterative analysis using the exponential diode model**
3. Graphical analysis using a load line
4. The ideal diode model
5. None of these

* Diodes can be used to limit how low the magnitude of a signal can go.

**FALSE**

* Diode limiters are used to control the gain of a circuit after the diodes turn on.

**TRUE**

* One of the most useful applications for diodes is in DC power supplies, which convert an AC input voltage into a DC output voltage.

**TRUE**

* The filter capacitor must be twice as large in a full-wave rectifier than in a half-wave rectifier to obtain the same ripple voltage.

**FALSE**

* In a power supply a large filter capacitor is typically used to smooth out the pulses from the rectifier to create a nearly constant output voltage, with only small variations called ripple.

**TRUE**

* The size of the ripple voltage at the output of a power supply filter capacitor is directly proportional to the size of the filter capacitor used.

**FALSE**

* The Constant Voltage diode model provides a good compromise between accuracy and ease of use when analyzing diode circuits.

**TRUE**

* A Full Wave Rectifier allows both the positive and negative peaks of the input sine wave through to the output.

**TRUE**

* In a DC Restorer circuit, a diode typically clamps the output voltage as it tries to move in one direction, and prevents it from going much past ground.

**TRUE**

* In a Full-wave rectifier which uses a center-tapped transformer, the minimum breakdown voltage required for the diodes is :

1. None of these
2. The peak input voltage
3. The peak-to-peak input voltage
4. **The peak-to-peak input voltage minus 1 diode drop**
5. The peak input voltage minus 1 diode drop

* Clamped Capacitor circuits can be used to restore DC values to AC coupled signals.

**TRUE**

* The size of the ripple voltage at the output of a power supply filter capacitor is inversely proportional to the size of the current supplied to the load.

**FALSE**

* Center-tapped transformers are often used in power supplies instead of bridge rectifiers to lower cost.

**FALSE**

* The Exponential diode model provides the best accuracy when analyzing diode circuits, but requires an iterative numerical approach to solve the nonlinear equations involved.

**TRUE**

* In a Half-wave rectifier without a filter capacitor, the minimum breakdown voltage required for the diodes is :

1. **The peak input voltage**
2. The peak input voltage minus 1 diode drop
3. The peak-to-peak input voltage
4. The peak-to-peak input voltage minus 1 diode drop
5. None of these

* Clamped Capacitor circuits can be used to restore AC values to DC coupled signals.

**FALSE**

* Superposition can be used to analyze nonlinear devices such as diodes as long as the variations around the bias point are kept small enough.

**TRUE**

* In a Full-wave rectifier which uses a diode bridge, the minimum breakdown voltage required for the diodes is :

1. The peak-to-peak input voltage
2. **The peak input voltage minus 1 diode drop**
3. The peak-to-peak input voltage minus 1 diode drop
4. The peak input voltage
5. None of these

* In the small-signal equivalent for a circuit containing a reverse biased Zener diode, the DC battery is used to model the diode’s reverse breakdown voltage at low current levels.

**TRUE**

* The Peak Inverse Voltage required for the diodes in a bridge rectifier is only about half of that required for a full wave rectifier which uses a center-tapped transformer.

**TRUE**

* Diodes can be used to limit how high the magnitude of a signal can go.

**TRUE**

* When performing a Load Line analysis on a diode circuit to find the bias point, the operating point for the diode is where the linear equation for the circuit and the diode’s nonlinear I-V characteristic curve both cross the X-axis on the plot.

**FALSE**

* Which of these circuits requires the diodes used to have the lowest peak inverse voltage rating?

1. **Full-wave rectifiers using a bridge rectifier**
2. Same for all of these
3. Half-wave rectifiers without a filter capacitor
4. Full-wave rectifiers using a center-tapped transformer
5. Impossible to determine

* In order to avoid problems with thermal runaway, diodes are usually biased at a constant voltage instead of with a constant current.

**FALSE**

* The incremental resistance for a Zener diode is used to model how much the voltage across the forward biased diode increases as the forward current flowing through it increases.

**FALSE**

* Line regulation is a measure of how much a reference voltage changes as the input supply voltage changes.

**TRUE**

* The Peak Inverse Voltage required for the diodes in a full wave rectifier which uses a center-tapped transformer is only about half of that required for a bridge rectifier.

**FALSE**

* A large enough piece of anything nonlinear looks linear.

**FALSE**

* Which of the following will give the least accurate results when analyzing diode circuits?

1. **The ideal diode model**
2. Iterative analysis using the exponential diode model
3. The constant voltage drop diode model
4. None of these
5. Graphical analysis using a load line

* Once a Zener diode breaks down in the reverse direction, the current through it only changes slightly as the voltage across it varies.

**FALSE**

* In a DC Restorer circuit, a diode typically clamps the output voltage as it tries to move in one direction, and prevents it from going much past the peak input voltage.

**FALSE**

* The voltage across a forward biased silicon diode will change by about +2mV/°C as temperature changes.

**FALSE**

* Which of the following circuits is NOT part of a typical DC power supply?

1. A diode rectifier
2. A voltage regulator
3. A power transformer
4. **A high pass filter**
5. None of these

* When a small reverse bias voltage is applied across a diode, the diode only conducts a small forward current called the saturation current.

**FALSE**

* Which of the following is NOT true for the small-signal resistance of a forward biased diode?

1. The small-signal resistance of a diode decreases as the bias current increases
2. None of these
3. **The small-signal resistance of a diode models the resistance of the silicon used to build the diode**
4. The small-signal resistance of a diode can be measured from the slope of the diode I-V curve
5. The small-signal resistance of a diode increases as the temperature increases

* The output voltage of a Voltage Doubler circuit is about twice the peak value of the input voltage.

**TRUE**

* Diode limiters can be used to make a square wave look more like a sine wave, which is useful in communications circuits.

**FALSE**

* Load regulation is a measure of how much a reference voltage changes as the load current changes.

**TRUE**

* For a Half Wave Rectifier the diode must be able to handle a Peak Inverse Voltage equal to nearly twice the peak of the input voltage.

**FALSE**

* In a power supply a transformer is typically used to reduce the high line voltage to a more useful, lower value.

**TRUE**

* If a diode at 300°K with a constant bias current of 100μA has a forward voltage of 700mV across it, what will the voltage drop across this same diode be if the bias current is increased to 1mA?

1. 640mV
2. **760mV**
3. 580mV
4. 820mV
5. None of these

* In a power supply a large filter capacitor is typically used to smooth out the pulses from the rectifier to create a constant output voltage which doesn’t vary over time.

**FALSE**

* The peak current which flows in the rectifier diodes for a power supply is often much smaller than the current supplied to the load.

**FALSE**

* In a DC Restorer circuit, a diode forces a capacitor to charge up to either the positive or negative peak of the input signal.

**TRUE**

* In the small-signal equivalent for a circuit containing a forward biased diode, the diode is replaced by it’s small-signal resistance which is proportional to the bias current.

**FALSE**

* The incremental resistance for a Zener diode is the reciprocal of the slope of the diode’s I-V characteristic curve as the reverse voltage across the diode increases above the diode’s reverse breakdown voltage.

**TRUE**

* If a diode at 300°K with a constant bias current of 1mA has a forward voltage of 700mV across it, what will the voltage drop across this same diode be if the bias current is decreased to 10μA?

1. 640mV
2. 820mV
3. **580mV**
4. 760mV
5. None of these

* If a diode at 300°K with a constant bias current of 1mA has a forward voltage of 700mV across it, what will the voltage drop across this same diode be if the bias current is decreased to 100μA?

1. **640mV**

* Once a Zener diode breaks down in the reverse direction, the voltage across it only changes slightly as the current through it varies.

**TRUE**

* The size of the ripple voltage at the output of a power supply filter capacitor is inversely proportional to the frequency of the input sine wave.

**TRUE**

* Using a larger filter capacitor in a power supply will result in lower ripple, but cost more.

**TRUE**

* In a power supply diodes are typically used to rectify the AC input voltage, which means converting a unipolar sine wave into a series of bipolar pulses.

**FALSE**

* For a Half Wave Rectifier the diode must be able to handle a Peak Inverse Voltage equal to nearly the peak of the input voltage.

**TRUE**

* Linear circuit analysis techniques can be applied to nonlinear circuits as long as the variations around the bias point are kept small enough.

**TRUE**

* The average current which flows in the rectifier diodes for a power supply is typically about twice the peak current which flows in these same rectifier diodes.

**FALSE**

* The size of the ripple voltage at the output of a power supply filter capacitor is directly proportional to the frequency of the input sine wave.

**FALSE**

* When a small reverse bias voltage is applied across a diode, the diode only conducts a small reverse current called the saturation current.

**TRUE**

* Load regulation is a measure of how much a reference voltage changes as the input supply voltage changes.

**FALSE**

* The size of the ripple voltage at the output of a power supply filter capacitor is directly proportional to the period of the input sine wave.

**TRUE**

* Using a larger filter capacitor in a power supply will result in both lower ripple and lower cost.

**FALSE**

# PRACTICE QUIZ 05

* What happens to the gate capacitance of a MOSFET biased with |Vgs| > |Vt| as the gate oxide thickness decreases?

1. The capacitance decreases
2. **The capacitance increases**
3. None of these
4. Impossible to determine
5. The capacitance doesn't change

* When |Vgs| > |Vt| for a PMOS FET the silicon surface directly beneath the gate oxide changes from n-type to p-type as holes are attracted to the surface.

**TRUE**

* The gate-to-channel voltage in a saturated NMOS FET is :

1. None of these
2. **Higher at the source end of the channel**
3. Impossible to determine
4. Higher at the drain end of the channel
5. The same everywhere in the channel

* The slope of the Id versus Vds curve for a MOSFET in saturation is zero.

**FALSE**

* Which of the following is true for a PMOS FET?

1. The body is doped N-
2. **All of these**
3. The drain and source are doped P+
4. The channel is formed by attracting holes to the surface
5. The threshold voltage is negative

* Which of the following is true for a PMOS FET?

1. None of these
2. The channel is formed by attracting electrons to the surface
3. The drain and source are doped N+
4. **The body is doped N-**
5. The threshold voltage is positive

* Which of the following is true for a PMOS FET?

1. All of these
2. The body is doped P-
3. **The drain and source are doped P+**
4. The channel is formed by attracting electrons to the surface
5. The threshold voltage is positive

* Which of the following is true for a PMOS FET?

1. The body is doped P-
2. **The channel is formed by attracting holes to the surface**
3. The drain and source are doped N+
4. The threshold voltage is positive
5. None of these

* Which of the following is true for a PMOS FET?

1. The drain and source are doped N+
2. **The threshold voltage is negative**
3. The channel is formed by attracting electrons to the surface
4. The body is doped P-
5. All of these

* Which of the following is true for a PMOS FET?

1. The threshold voltage is positive
2. The drain and source are doped N+
3. The channel is formed by attracting electrons to the surface
4. **None of these**
5. The body is doped P-

* To keep the parasitic PN junction diodes turned off in a CMOS process, the P-substrate should be connected to the lowest supply voltage used on the IC.

**TRUE**

* What happens to the gate-to-channel voltage in a saturated NMOS FET as you move from source to drain?

1. **The gate-to-channel voltage decreases**
2. Impossible to determine
3. The gate-to-channel voltage doesn't change
4. The gate-to-channel voltage increases
5. None of these

* The saturation region of operation for a MOSFET is when |Vgs| > |Vt| so that the FET is turned on, and |Vds| < |Vgs| - |Vt| so that the channel is pinched off near the drain.

**FALSE**

* The capacitance of a MOSFET’s gate decreases as the thickness of the gate oxide increases.

**TRUE**

* Compared to the device transconductance for a PMOS FET, the device transconductance for an NMOS FET is :

1. **Impossible to determine**
2. Same
3. None of these
4. Smaller
5. Larger

* As Vds is increased above Vgs – Vt for a saturated NMOS FET :

1. The channel becomes “pinched-off” near the drain
2. **All of these**
3. The voltage across the channel stays the same
4. The capacitance of the drain PN junction gets smaller
5. The depletion region around the drain gets wider

* As Vds is increased above Vgs – Vt for a saturated NMOS FET :

1. **The capacitance of the drain PN junction gets smaller**
2. All of these
3. The voltage across the channel increases
4. The depletion region around the drain gets narrower
5. The channel becomes “pinched-off” near the source

* As Vds is increased above Vgs – Vt for a saturated NMOS FET :

1. The capacitance of the drain PN junction gets larger
2. The channel becomes “pinched-off” near the source
3. The depletion region around the drain gets narrower
4. **The voltage across the channel stays the same**
5. None of these

* As Vds is increased above Vgs – Vt for a saturated NMOS FET :

1. All of these
2. The voltage across the channel increases
3. **The depletion region around the drain gets wider**
4. The channel becomes “pinched-off” near the source
5. The capacitance of the drain PN junction gets larger

* As Vds is increased above Vgs – Vt for a saturated NMOS FET :

1. The capacitance of the drain PN junction gets larger
2. **The channel becomes “pinched-off” near the drain**
3. The depletion region around the drain gets narrower
4. The voltage across the channel increases
5. None of these

* As Vds is increased above Vgs – Vt for a saturated NMOS FET :

1. The depletion region around the drain gets narrower
2. The voltage across the channel increases
3. The capacitance of the drain PN junction gets larger
4. **None of these**
5. The channel becomes “pinched-off” near the source

* The drain current for a triode MOSFET increases linearly at first for small values of Vds, but then increases more slowly as Vds is increased further because the resistance of the channel near the drain end goes up as Vds is increased.

**TRUE**

* What happens to the amount of charge on the gate of a MOSFET biased with |Vgs| > |Vt| as the |Vgs| decreases?

1. **The amount of charge decreases**
2. The amount of charge doesn't change
3. None of these
4. The amount of charge increases
5. Impossible to determine

* The “overdrive voltage” for a MOSFET is given by |Vov| = |Vgs| – |Vt|.

**TRUE**

* If a PMOS FET is biased with |Vgs| > |Vt| and |Vds| > |Vgs| – |Vt|, the device is in :

1. Triode
2. **Saturation**
3. None of these
4. Sub-threshold
5. Cutoff

* The triode region of operation for a MOSFET is when |Vgs| > |Vt| so that the FET is turned on, and |Vds| > |Vgs| - |Vt| so that the channel connects the drain and the source.

**FALSE**

* To keep the parasitic PN junctions in a CMOS process turned off, which of the following must be done?

1. None of these
2. The P-substrate must be connected to the highest voltage used on the integrated circuit
3. The sources of the NMOS FETs must be connected to the lowest voltage used on the integrated circuit
4. **The N-wells must be connected to the highest voltage used on the integrated circuit**
5. The sources of the PMOS FETs must be connected to the highest voltage used on the integrated circuit

* To keep the parasitic PN junctions in a CMOS process turned off, which of the following must be done?

1. The sources of the PMOS FETs must be connected to the highest voltage used on the integrated circuit
2. The sources of the NMOS FETs must be connected to the lowest voltage used on the integrated circuit
3. **The P-substrate must be connected to the lowest voltage used on the integrated circuit**
4. None of these
5. The N-wells must be connected to the lowest voltage used on the integrated circuit

* To keep the parasitic PN junctions in a CMOS process turned off, which of the following must be done?

1. The sources of the PMOS FETs must be connected to the highest voltage used on the integrated circuit
2. **None of these**
3. The sources of the NMOS FETs must be connected to the lowest voltage used on the integrated circuit
4. The P-substrate must be connected to the highest voltage used on the integrated circuit
5. The N-wells must be connected to the lowest voltage used on the integrated circuit

* The flow of current between the drain and source of a MOSFET is controlled using electric fields.

**TRUE**

* If an NMOS FET is biased with Vgs slightly < Vt and Vds > Vgs – Vt, the device is in :

1. Triode
2. **Sub-threshold**
3. Saturation
4. None of these
5. Cutoff

* For a MOSFET operating in saturation, the channel extends all the way from the source to the drain.

**FALSE**

* The capacitance of a MOSFET’s gate increases as the width of the gate increases.

**TRUE**

* If an NMOS FET is biased with Vgs > Vt and Vds < Vgs – Vt, the device is in :

1. **Triode**
2. None of these
3. Sub-threshold
4. Saturation
5. Cutoff

* The cutoff region of operation for a MOSFET is when |Vgs| < |Vt| so that the FET is turned off and no channel exists.

**TRUE**

* When FETs are built, parasitic PN junction diodes are also created that must be kept reverse biased at all times.

**TRUE**

* What happens to the channel resistance of a triode MOSFET as W/L increases?

1. The resistance increases
2. **The resistance decreases**
3. Impossible to determine
4. None of these
5. The resistance doesn't change

* The triode region of operation for a MOSFET is when |Vgs| > |Vt| so that the FET is turned on, and |Vds| < |Vgs| - |Vt| so that the channel connects the drain and the source.

**TRUE**

* PMOS FETs use P+ doped source and drain diffusions in a P-type substrate.

**FALSE**

* The gate-to-drain voltage in a saturated NMOS FET is :

1. Greater than the threshold voltage
2. Greater than the gate-to-source voltage
3. Greater than the gate-to-channel voltage
4. All of these
5. **None of these**

* The Id versus Vds curve for a MOSFET in saturation is nearly flat.

**TRUE**

* Compared to the process transconductance for a PMOS FET, the process transconductance for an NMOS FET is :

1. **Larger**
2. Smaller
3. Impossible to determine
4. Same
5. None of these

* Key parameters which circuit designers use to control how a MOSFET operates is the width and length of the source.

**FALSE**

* Most things in nature just turn off abruptly like a light switch.

**FALSE**

* What happens to the gate capacitance of a MOSFET biased with |Vgs| > |Vt| as the gate oxide thickness increases?

1. None of these
2. The capacitance doesn't change
3. **The capacitance decreases**
4. The capacitance increases
5. Impossible to determine

* The amount of charge stored on a MOSFET’s gate capacitance is directly proportional to |Vgs| – |Vt|.

**TRUE**

* As |Vds| is increased above |Vgs| – |Vt| for a saturated PMOS FET :

1. The channel becomes “pinched-off” near the drain
2. The voltage across the channel stays the same
3. **All of these**
4. The capacitance of the drain PN junction gets smaller
5. The depletion region around the drain gets wider

* As |Vds| is increased above |Vgs| – |Vt| for a saturated PMOS FET :

1. All of these
2. **The voltage across the channel stays the same**
3. The channel becomes “pinched-off” near the source
4. The capacitance of the drain PN junction gets larger
5. The depletion region around the drain gets narrower

* As |Vds| is increased above |Vgs| – |Vt| for a saturated PMOS FET :

1. The depletion region around the drain gets narrower
2. The channel becomes “pinched-off” near the source
3. The voltage across the channel increases
4. None of these
5. **The capacitance of the drain PN junction gets smaller**

* As |Vds| is increased above |Vgs| – |Vt| for a saturated PMOS FET :

1. The voltage across the channel increases
2. **The depletion region around the drain gets wider**
3. The capacitance of the drain PN junction gets larger
4. The channel becomes “pinched-off” near the source
5. None of these

* As |Vds| is increased above |Vgs| – |Vt| for a saturated PMOS FET :

1. The voltage across the channel increases
2. **None of these**
3. The capacitance of the drain PN junction gets larger
4. The depletion region around the drain gets narrower
5. The channel becomes “pinched-off” near the source

* MOSFETs are often referred to as “square law devices” because the drain current increases proportional to the square root of (|Vgs| - |Vt|) in saturation.

**FALSE**

* What happens to the gate capacitance of a MOSFET biased with |Vgs| > |Vt| as the |Vgs| increases?

1. Impossible to determine
2. **The capacitance doesn't change**
3. None of these
4. The capacitance increases
5. The capacitance decreases

* The process transconductance for a MOSFET, k’ , is directly proportional to the gate oxide capacitance, the carrier mobility, and the W/L of the FET.

**FALSE**

* For large values of Vds the Id vs Vds curve for a MOSFET is linear, and looks just like a resistor.

**FALSE**

* Key parameters which circuit designers use to control how a MOSFET operates is the width and length of the gate.

**TRUE**

* As Vds is increased above Vgs – Vt in a saturated NMOS FET, the voltage across the channel :

1. Increases
2. None of these
3. **Stays constant**
4. Decreases
5. Impossible to determine

* The saturation region of operation for a MOSFET is when |Vgs| > |Vt| so that the FET is turned on, and |Vds| > |Vgs| - |Vt| so that the channel is pinched off near the drain.

**TRUE**

* Which of the following is true for an NMOS FET?

1. **All of these**
2. The drain and source are doped N+
3. The threshold voltage is positive
4. The body is doped P-
5. The channel is formed by attracting electrons to the surface

* Which of the following is true for an NMOS FET?

1. The channel is formed by attracting holes to the surface
2. The threshold voltage is negative
3. None of these
4. The body is doped N-
5. **The drain and source are doped N+**

* Which of the following is true for an NMOS FET?

1. All of these
2. **The body is doped P-**
3. The channel is formed by attracting holes to the surface
4. The drain and source are doped P+
5. The threshold voltage is negative

* Which of the following is true for an NMOS FET?

1. The drain and source are doped P+
2. All of these
3. **The channel is formed by attracting electrons to the surface**
4. The body is doped N-
5. The threshold voltage is negative

* Which of the following is true for an NMOS FET?

1. The channel is formed by attracting holes to the surface
2. None of these
3. The body is doped N-
4. The drain and source are doped P+
5. **The threshold voltage is positive**

* Which of the following is true for an NMOS FET?

1. The channel is formed by attracting holes to the surface
2. **None of these**
3. The threshold voltage is negative
4. The body is doped N-
5. The drain and source are doped P+

* When Vgs > Vt for an NMOS FET the silicon surface directly beneath the gate oxide changes from p-type to n-type as electrons are attracted to the surface.

**TRUE**

* For a MOSFET in saturation, as |Vds| increases the length of the channel:

1. Stays the same
2. **Decreases**
3. Increases
4. Impossible to determine
5. None of these

* A simple approximation for the minimum |Vds| required in order for a MOSFET to be in saturation is |Vds-sat| = |Vgs| - |Vt|.

**TRUE**

* To keep the parasitic PN junction diodes turned off in a CMOS process, the P-substrate should be connected to the highest supply voltage used on the IC.

**FALSE**

* As Vds is increased above Vgs – Vt in a saturated NMOS FET, which of the following increases ?

1. The length of the channel
2. The width of the depletion region surrounding the source PN junction
3. The voltage across the channel
4. All of these
5. **The width of the depletion region surrounding the drain PN junction**

* The resistance of a MOSFET operating in triode decreases as the W/L of the MOSFET increases.

**TRUE**

* Compared to the device transconductance for an NMOS FET, the device transconductance for a PMOS FET is :

1. Same
2. Smaller
3. None of these
4. **Impossible to determine**
5. Larger

* NMOS FETs use N+ doped source and drain diffusions in a P-type substrate.

**TRUE**

* The drain current for a triode MOSFET increases linearly at first for small values of Vds, but then increases more slowly as Vds is increased further because the resistance of the channel near the source end goes up as Vds is increased.

**FALSE**

* To keep the parasitic PN junction diodes turned off in a CMOS process, the N-wells should be connected to the highest supply voltage used on the IC.

**TRUE**

* What happens to the gate-to-channel voltage in a triode NMOS FET as you move from source to drain?

1. **Impossible to determine**
2. The gate-to-channel voltage doesn't change
3. The gate-to-channel voltage decreases
4. The gate-to-channel voltage increases
5. None of these

* A MOSFET enters the saturation region of operation when the gate-to-channel voltage at the drain end of the channel drops below the threshold voltage.

**TRUE**

* Compared to the mobility of holes in silicon, the mobility of electrons is :

1. **Larger**
2. Smaller
3. None of these
4. The same
5. Impossible to determine

* When |Vgs| > |Vt| for a MOSFET the gate forms a parallel-plate capacitor between the gate and the channel.

**TRUE**

* If a PMOS FET is biased with |Vgs| slightly < |Vt| and |Vds| < |Vgs| – |Vt|, the device is in :

1. Triode
2. Saturation
3. None of these
4. Cutoff
5. **Sub-threshold**

* The Id versus Vds curve for a MOSFET in triode is nearly flat.

**FALSE**

* What happens to the gate capacitance of a MOSFET biased with |Vgs| > |Vt| as the gate length decreases?

1. The capacitance doesn't change
2. None of these
3. Impossible to determine
4. **The capacitance decreases**
5. The capacitance increases

* The flow of current between the drain and source of a MOSFET is controlled by varying the gate current.

**FALSE**

* As Vds is increased above Vgs – Vt in a saturated NMOS FET, the voltage across the depletion region surrounding the drain PN junction :

1. Impossible to determine
2. **Increases**
3. None of these
4. Decreases
5. Stays constant

* The resistance of a MOSFET operating in triode decreases as |Vgs| - |Vt| increases.

**TRUE**

* When Vgs > Vt for an NMOS FET the silicon surface directly beneath the gate oxide changes from n-type to p-type as holes are attracted to the surface.

**FALSE**

* For |Vgs| < |Vt| the drain current for a MOSFET actually drops linearly as |Vgs| is decreased rather than just suddenly going to zero.

**FALSE**

* The capacitance of a MOSFET’s gate increases as the length of the gate increases.

**TRUE**

* PMOS FETs use P+ doped source and drain diffusions in a N-type substrate.

**TRUE**

* What happens to the channel resistance of a triode MOSFET as W/L decreases?

1. The resistance doesn't change
2. None of these
3. Impossible to determine
4. The resistance decreases
5. **The resistance increases**

* MOSFETs are often referred to as “square law devices” because the drain current increases proportional to the square of (|Vgs| - |Vt|) in saturation.

**TRUE**

* The process transconductance for a MOSFET, k’ , is directly proportional to both the gate oxide capacitance and the carrier mobility, but doesn’t depend on the W/L of the FET.

**TRUE**

* For a MOSFET operating in triode, the channel extends all the way from the source to the drain.

**TRUE**

* What happens to the amount of charge on the gate of a MOSFET biased with |Vgs| > |Vt| as the |Vgs| increases?

1. **The amount of charge increases**
2. The amount of charge doesn't change
3. None of these
4. Impossible to determine
5. The amount of charge decreases

* If a PMOS FET is biased with |Vgs| > |Vt| and |Vds| < |Vgs| – |Vt|, the device is in :

1. Saturation
2. **Triode**
3. Cutoff
4. None of these
5. Sub-threshold

* A MOSFET operating in subthreshold still conducts a small amount of drain current even though |Vgs| is greater than |Vt|.

**FALSE**

* What happens to the gate capacitance of a MOSFET biased with |Vgs| > |Vt| as the gate width increases?

1. The capacitance decreases
2. **The capacitance increases**
3. The capacitance doesn't change
4. Impossible to determine
5. None of these

* The capacitance of a MOSFET’s gate increases as the thickness of the gate oxide increases.

**FALSE**

* What happens to the channel resistance of a triode MOSFET as |Vgs| – |Vt| decreases?

1. Impossible to determine
2. None of these
3. **The resistance increases**
4. The resistance doesn't change
5. The resistance decreases

* The amount of charge that is in the channel of a MOSFET at any particular point in the channel is inversely proportional to the gate-to-channel voltage at that point in the channel.

**FALSE**

* Compared to the mobility of electrons in silicon, the mobility of holes is :

1. None of these
2. **Smaller**
3. Larger
4. The same
5. Impossible to determine

* When |Vgs| < |Vt| for a MOSFET the gate forms a parallel-plate capacitor between the gate and the channel.

**FALSE**

* The gate-to-drain voltage in a triode NMOS FET is :

1. Greater than the gate-to-source voltage
2. **Greater than the threshold voltage**
3. None of these
4. Greater than the gate-to-channel voltage
5. All of these

* The Id versus Vds curve for a MOSFET is linear even for large values of |Vds|, as long as |Vds| < |Vds-sat|.

**FALSE**

* The length of the channel in a MOSFET is the distance between the drain and the source.

**TRUE**

* If an NMOS FET is biased with Vgs > Vt and Vds > Vgs – Vt, the device is in :

1. Sub-threshold
2. Cutoff
3. None of these
4. Triode
5. **Saturation**

* The threshold voltage for an NMOS FET is positive.

**TRUE**

* For a MOSFET in saturation, changes in Vds have only a small effect on the drain current because the channel stops being pinched off at the drain end as |Vds| is increased.

**FALSE**

* If an NMOS FET is biased with Vgs << Vt and Vds < Vgs – Vt, the device is in :

1. **Cutoff**
2. None of these
3. Saturation
4. Sub-threshold
5. Triode

* For a MOSFET in triode, the amount of charge in the channel at the drain end is approximately zero.

**FALSE**

* When |Vgs| > |Vt| for a PMOS FET the silicon surface directly beneath the gate oxide changes from p-type to n-type as electrons are attracted to the surface.

**FALSE**

* As |Vds| is increased above |Vgs| – |Vt| for a saturated PMOS FET :

1. The voltage across the channel increases
2. The depletion region around the drain gets narrower
3. **The channel becomes “pinched-off” near the drain**
4. The capacitance of the drain PN junction gets larger
5. All of these

* The resistance of a MOSFET operating in triode increases as |Vgs| - |Vt| increases.

**FALSE**

* Compared to the process transconductance for an NMOS FET, the process transconductance for a PMOS FET is :

1. Impossible to determine
2. None of these
3. **Smaller**
4. Larger
5. Same

* The device transconductance for a MOSFET, β , is directly proportional to both the gate oxide capacitance and the carrier mobility, but doesn’t depend on the W/L of the FET.

**FALSE**

* A simple approximation for the maximum |Vds| required in order for a MOSFET to be in saturation is |Vds-sat| = |Vgs| - |Vt|.

**FALSE**

* The width of the channel in a MOSFET is the distance between the drain and the source.

**FALSE**

* Most things in nature don’t just turn off abruptly like a light switch.

**TRUE**

* The “overdrive voltage” for a MOSFET is given by |Vov| = |Vds| – |Vt|.

**FALSE**

* If a PMOS FET is biased with |Vgs| << |Vt| and |Vds| < |Vgs| – |Vt|, the device is in :

1. Triode
2. **Cutoff**
3. Sub-threshold
4. None of these
5. Saturation

* For a MOSFET in saturation, the amount of charge in the channel at the drain end is approximately zero.

**TRUE**

* NMOS FETs use N+ doped source and drain diffusions in a N-type substrate.

**FALSE**

* The cutoff region of operation for a MOSFET is when |Vgs| > |Vt| so that the FET is turned off and no channel exists.

**FALSE**

* The threshold voltage of a MOSFET is the amount of voltage that must be applied between the drain and the source in order for a channel to be formed between the gate and the source.

**FALSE**

* What happens to the current in a saturated MOSFET as |Vds| increases above |Vgs| – |Vt| ?

1. Impossible to determine
2. The current decreases
3. **The current increases**
4. The current doesn't change
5. None of these

* For a MOSFET operating in triode, the channel is pinched off near the drain.

**FALSE**

* The capacitance of a MOSFET’s gate decreases as the thickness of the gate oxide decreases.

**FALSE**

* For a MOSFET operating in saturation, the channel is pinched off near the drain.

**TRUE**

* The device transconductance for a MOSFET, β , is directly proportional to the gate oxide capacitance, the carrier mobility, and the W/L of the FET.

**TRUE**

* What happens to the channel resistance of a triode MOSFET as |Vgs| – |Vt| increases?

1. None of these
2. The resistance doesn't change
3. The resistance increases
4. Impossible to determine
5. **The resistance decreases**

* A MOSFET enters the saturation region of operation when the gate-to-channel voltage at the drain end of the channel rises above the threshold voltage.

**FALSE**

* Modern CMOS processes use an N-type silicon substrate with NMOS FETs built in P-wells.

**FALSE**

* For small values of Vds the Id vs Vds curve for a MOSFET is linear, and looks just like a resistor.

**TRUE**

* Modern CMOS processes use a P-type silicon substrate with PMOS FETs built in N-wells.

**TRUE**

* A MOSFET operating in subthreshold still conducts a small amount of drain current even though |Vgs| is less than |Vt|.

**TRUE**

* When FETs are built, parasitic PN junction diodes are also created that must be kept forward biased at all times.

**FALSE**

* The resistance of a MOSFET operating in triode increases as the W/L of the MOSFET increases.

**FALSE**

* To keep the parasitic PN junction diodes turned off in a CMOS process, the N-wells should be connected to the lowest supply voltage used on the IC.

**FALSE**

* For |Vgs| < |Vt| the drain current for a MOSFET actually drops exponentially as |Vgs| is decreased rather than just suddenly going to zero.

**TRUE**

* The amount of charge stored on a MOSFET’s gate capacitance is directly proportional to |Vds| – |Vt|.

**FALSE**

* For a MOSFET with Vds > 0, the gate-to-channel voltage is higher at the drain end of the channel than at the source end.

**FALSE**

* The threshold voltage for an NMOS FET is negative.

**FALSE**

* For a MOSFET with Vds > 0, the gate-to-channel voltage is lower at the drain end of the channel than at the source end.

**TRUE**

# The threshold voltage for a PMOS FET is negative.

**TRUE**

* For a MOSFET in saturation, changes in Vds have only a small effect on the drain current because the channel is pinched off at the drain end.

**TRUE**

* The capacitance of a MOSFET’s gate decreases as the length of the gate increases.

**FALSE**

* The amount of charge that is in the channel of a MOSFET at any particular point in the channel is directly proportional to the gate-to-channel voltage at that point in the channel.

**TRUE**

* The threshold voltage of a MOSFET is the amount of voltage that must be applied between the gate and the source in order for a channel to be formed between the drain and the source.

**TRUE**

* The slope of the Id versus Vds curve for a MOSFET in saturation is very small.

**TRUE**

* The capacitance of a MOSFET’s gate increases as the thickness of the gate oxide decreases.

**TRUE**

* The Id versus Vds curve for a MOSFET is linear for small values of |Vds| << |Vds-sat|.

**TRUE**

* The threshold voltage for a PMOS FET is positive.

**FALSE**

* The capacitance of a MOSFET’s gate increases as the area of the gate increases.

**TRUE**

* The capacitance of a MOSFET’s gate decreases as the width of the gate increases.

**FALSE**

* The capacitance of a MOSFET’s gate decreases as the area of the gate increases.

FALSE